Performance Improvement of ISM 5.8 GHz Transceivers

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Dedicated to my beloved wife and son

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List of Abbreviations

AC	Alternative current
ACPR	Adjacent Channel Power Ratio
ADC	Analog-to-digital converter
ADS	Advanced designed system
AFL	Active feedback lineariser
AIAs	Active integrated antennas
AM-AM	Amplitude modulation-amplitude modulation
AM-PM	Amplitude modulation-phase modulation
CDMA	Code-Division Multiple Access
CG	Common gate
CMRC	Compact microstrip resonant cell
CMOS	Complementary metal-oxide-semiconductor
CPW	Coplanar waveguide
CRSA	Circular ring slot antenna
CS	Common source
DC	Direct current
DGS	Defected ground structure
EDGE	Enhanced Data for Global Evolution
EVM	Error Vector Magnitude
FBW	Fractional bandwidth
FDD	Frequency division duplexing
FET	Field-effect transistor
FOM	Figure of merit
GMSK	Gaussian Minimum Shift Keying
GSM	Global System for Mobile Communication
HFSS	High Frequency Electromagnetic Field Simulation Software
HF	Harmonic supression
IBFD	In-Band Full-Duplex
IMD3	Third-order Intermodulation Distortion
IMD5	Fifth-order intermodulation distortion
IoT	Internet of Things
IP3	Third-order Intercept Point
iPDK	Process Design Kit
ISM	Industrial, Scientific and Medical
LNA	Low noise amplifier
LPW	Low pass filter
MGTR	Multi-gated transistor
MIM	Metal-insulator-metal
MMIC	Monolithic microwave integrated circuit
NMOS	Metal-oxide-semiconductor
OFDM	Orthogonal Frequency-Division Multiplexing
PA	Power amplifier
PAE	Power-added efficiency
PARP	Peak-to-average power ratio
PBG	Photonic bandgap
PCB	Printed circuit board

PLL	Phased lock loop
PSD	Power spectral density
QAM	Quadrature amplitude modulation
RC	Resistor capacitor
RF	Radio frequency
RFID	Radio frequency identification
RMS	Root mean square
RX	Receiver
SI	Self-interference
SIC	Self-interference cancellation
SIR	Stepped-impedance-resonator
SMA	Surface mount adaptor
TLT	Tranmission line transformer
TSMC	Taiwan Semiconductor Manufacturing Company
TX	Transmitter
VCO	Voltage-controlled oscillator
VSWR	voltage-standing-wave-ratio
WLAN	Wireless Local Area Network

List of Symbols

μ	Mobility of the majority carriers in channel
Cox	Capacitance of the oxide layer
Vth	Threshold voltage
W	Channel width
L	Channel length
$I0$	Drain-source current at threshold voltage
kB	Boltzmann's constant (=1.38x10-3J/K)
T	Temperature in Kelvin
OP_{1dB}	Output power one dB compression point
P_{SAT}	Saturation output power
P_{OUT}	Output power
P_{IN}	Input power
P_{DC}	Direct current power consumption
K	Rowlett stability factor
S_{11}	Input return loss
S_{22}	Output return loss
S_{12}	Reverse transmission coefficient
S_{21}	Forward transmission coefficient
Δ	Delta
V_{GS}	Gate source voltage
V_{DD}	Supply voltage
V_{ref}	Reference voltage
V_{DS}	Drain source voltage
V_{DG}	Drain gate voltage
V_{TH}	Threshold voltage
V_{OUT}	Output voltage
V_{IN}	Input voltage
V_b	Bias voltage
g_m	Transconductance of transistor
$\mu_n C_{ox}$	Constant of the semiconductor technology
λ	One wavelength
P_i	Incident power
P_r	Reflected power
C_{21}	Coupling coefficient
Γ_L	Reflection coefficient
$x(t)$	Acos(wt) input signal fed to the gain stage
$y_1(t)$	Output signal at stage 1 of the two stage PA
$y_2(t)$	Output signal at stage 2 of the two stage PA
$A_{in,1dB}$	The input P1dB of the whole PA
C_{gs}	Non-linear gate-source capacitance
C_{ds}	Non-linear drain-source capacitance
C_{gd}	Non-linear gate-drain capacitance
I_{D0}	Drain current
$Out+$	Positive output
$Out-$	Negative output
$In+$	Positive input
$In-$	Negative input
K	Magnetic coupling coefficient
M	Mutual coupling
N	Turn ratio
ϕ_{12}	Magnetic flux from primary coil to secondary coil
ϕ_{21}	Magnetic flux from secondary coil to primary coil
V_1	Voltage in primary coil
V_2	Voltage in secondary coil
I_1	Current in primary coil
I_2	Current in secondary coil

L_1	Voltage in primary coil
L_2	Voltage in secondary coil
C_{i1}	Inter-stage matching capacitor at the 1st stage amplifier
C_{i2}	Inter-stage matching capacitor at the 1st stage amplifier
C_{m1}	Inter-stage matching capacitor between the 1st stage and the 2nd stage amplifiers
C_{m2}	Inter-stage matching capacitor between the 1st stage and the 2nd stage amplifiers
C_{o1}	Output serial capacitor at PA
C_{o2}	Output parallel capacitor at PA
R_{f1}	Feedback resistor at the 1st stage amplifier
C_{f1}	Feedback capacitor at the 1st stage amplifier
R_{f2}	Feedback resistor at the 2nd stage amplifier
C_{f2}	Feedback capacitor at the 2nd stage amplifier
C_{h1} to C_{h6}	Large capacitors for 2nd harmonic short circuit at the power amplifier circuits
M_1	The CS transistor of the 1st stage
M_2	The CG transistor of the 1st stage
M_3	The CS transistor of the 2nd stage
M_4	The CG transistor of the 2nd stage
R_{m1}	RF blocking signal for the bias voltage supply V_{B1} of the 1st stage
R_{m2}	RF blocking signal for the bias voltage supply V_{B2} of the 2nd stage
R_{p1}	Bias resistor at the PMOS lineariser
R_{p2}	Bias resistor at the PMOS lineariser
R_{p3}	Bias resistor at the PMOS lineariser
V_{B1}	Bias voltage of the 1st stage amplifier
V_{B2}	Bias voltage of the 2nd stage
V_{DD1}	Supply voltage for the 1st stage amplifier
V_{DD2}	Supply voltage for the 2nd stage amplifier
X_1	Input transmission-line transformer of the PA
X_2	Middle transmission-line transformer of the PA
X_3	Output transmission-line transformer of the PA
RF_IN	RF input signal
RF_OUT	RF output signal
Z (1,1)	Input impedance
Z (2,2)	Output impedance
Z (1,2)	Reverse impedance
Z (2,1)	Forward impedance
Q	Quality factor
J_{max}	Maximum DC current allowed per um of metal line width
V_S	Source voltage of a CMOS transistor
V_D	Drain voltage of a CMOS transistor
V_G	Gate voltage of a CMOS transistor
I_{DS}	Drain source current
V PMOS	Bias voltage for PMOS lineariser
I_1	Current of the 1st stage amplifier
I_2	Current of the 2nd stage amplifier
R_b	Equivalent resistance of bondwire
L_b	Equivalent inductance of bondwire
C_{pakage_pad}	Equivalent capacitance of bondwire at package site
C_{chip_pad}	Equivalent capacitance of bondwire at chip site
e_r	Relative dielectric constant
Z_s	Characteristic impedance of a slot line
R_A	Radiation resistor
λ_{effs}	Effective wavelength
e_{effs}	Effective dielectric constant
Z_{dgs}	Impedance of DGS

λ_{effd}	Effective wavelength of the DGS
β	Propagation constant
Z_{sl}	Characteristic impedance of slot line of DGS
θ_1	Electrical length of slotline 1 in a Stepped Impedance Resonator
θ_2	Electrical length of slotline 2 in a Stepped Impedance Resonator
K	Impedance ratio Z_2/Z_1 or coupling factor
n_S	Transformer's ratio
v_p	Velocity of the wave in a slotline
C_{MIM}	Metal-insulator-metal capacitor
C_g	Fringing capacitance
f_{max}	The highest operational frequency
a_e	Even mode incident wave
a_o	Odd mode incident wave
a_{sa}	Incident wave to slot A
a_{sb}	Incident wave to slot B
b_e	Even mode reflected wave
b_o	Odd mode reflected wave
b_{sa}	Reflected wave to slot A
b_{sb}	Reflected wave to slot B
C_{21}	Coupling coefficient from port 2 to port 2
S_{31}	S-parameter from port 1 to port 3
S_{23}	S-parameter from port 3 to port 2
S_{33}	Return loss of port 3
S_{21}	Coupling or isolation
Γ_L	Reflection coefficient of Port 3
C_{cpw}	Terminal capacitor at the end of a PCW
Z_{Ccpw}	Impedance of the C_{cpw}
$Z_{sl\text{-}ant}$	Impedance of stepped slot antenna
$Z_{st,o}$	Characteristic odd mode impedance
$Z_{st,e}$	Characteristic even mode impedance of the CPW
$\beta_{st,e}$	Even mode propagation constant
$\beta_{st,o}$	Odd mode propagation constant
$Z_{ant,e}$	Even mode impedance of slot antenna
$Z_{ant,o}$	Odd mode impedance of slot antenna

Statement of Authorship

Except where reference is made in the text of the thesis, this thesis contains no material published elsewhere or extracted in whole or in part from a thesis submitted for the award of any other degree or diploma.

No other person's work has been used without due acknowledgment in the main text of the thesis.

This thesis has not been submitted for the award of any degree or diploma in any other tertiary institution.

15/02/2021

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Abstract

This dissertation aims to improve important features of RF components for Internet of Things (IoT) applications including size, data rate, power consumption, and cost. To contribute to these objectives the research focusses on developing high linearity power amplifier (PA), new harmonic suppression antennas, and a full duplex antenna.

First, a highly linear cascode PA design for 5.8 GHz industrial, scientific, and medical (ISM) band is presented. The two-stage PA employs a differential topology to achieve high common-mode interference immunity along with an adaptive bias linearizing circuit without introducing any insertion loss. The design achieves high figure of merit in a small size with 1- dB compression point of the linearized PA improving by 2.6 dB compared to conventional designs.

Second, harmonic suppression antenna (HSA) designs for 5.8 GHz ISM band are presented where their out of band rejection capability offers area and cost efficiency when compared to approaches requiring filters. Two narrow slot antennas, a Double HSA and a Small Size Slot HSA are proposed using DGS and other harmonic suppression techniques resulting in reduced length and very strong rejection capability of 1 to 2 dB. For wideband applications covering whole of C band, a triangle slot antenna design with added DGS and thin microstrip line structures is presented which achieves improved bandwidth to 5.51 GHz while keeping the out-of-band return loss smaller than 1.2 dB (up to 26.5 GHz) and with maximum rejection of 33.8 dB.

Finally, a single-layered slot antenna system for 5.8 GHz ISM band is proposed for In-band full-duplex (IBFD) applications without the use of a coupler. High isolation is achieved by strong separation of even and odd mode feeds which are a microstrip-coupled coplanar waveguide and a microstrip T-junction power divider. The measured isolation between the two ports is about 50 dB across the bandwidth.

List of Publications

Accepted Journals:

[1] **Ngoc-Anh Nguyen**, Mohsen Radfar, Amir Ebrahimi, Vu-Duc Ngo, Aidin Bervan, Viet Hoang Le, and Aniruddha Desai, "Wideband Compact Triangle Slot Antenna with Out-Of-Band Rejection," *IEEE Antennas and Wireless Propagation Letters*, pp. 1-1, 2020, doi: 10.1109/LAWP.2020.2982177.

This paper discusses a wideband harmonic supersession antenna which can achieve better miniaturization and longer battery lifetime. In addition, the signal-to-noise ratio can be improved using this technique, leading to a higher data rate. In this paper, a novel antenna, which is needed in applications which require a large bandwidth, is proposed with a highly out-of-band rejection characteristic using a new combination of suppression techniques. This paper is discussed in Chapter 4 together with two other narrow band harmonic suppression antennas.

[2] **Ngoc-Anh Nguyen**, Viet Hoang Le, Nghia Nguyen-Trong, Mohsen Radfar, Amir Ebrahimi, Khoa Phan, and Aniruddha Desai, "A High-Isolation Slot Antenna for Full-Duplex Systems," *IEEE Transactions on Antennas and Propagation Communication,* 2020, doi: 10.1109/TAP.2020.3010959.

This paper is based around the design of a high-isolation antenna for in-band full-duplex communication, which is an attractive option for a high data rate due to its potential to double spectral efficiency. This work, which covers various aspects from antenna impedance matching to isolation improvement, is discussed in Chapter 5. This paper has been accepted for publication in 2021 in the IEEE Special Issue on Antennas and Propagation Aspects of In-Band Full-Duplex Applications.

Submitted Journals:

[3] Amir Nakhlestani, Mohsen Radfar, **Ngoc-Anh Nguyen**, Aniruddha Desai," Area-Efficient Single-Cell Charge-Pump using Virtual Diode Concept for Ultra-Low Power IoT and Sensory Applications," *IEEE Transactions on Very Large-Scale Integration Systems,* 2020.

The paper covers the design and implementation of an area-efficient charge-pump, where the performance satisfies the need for ultra-low power IoT and sensory applications.

[4] **Ngoc-Anh Nguyen**, Mohsen Radfar, Quang Diep Bui, Amir Nakhlestani, Shridevi Venkatesh Kaveri, Hoang Viet Le, Aniruddha Desai, "A low voltage RF 5.8 GHz Integrated CMOS Power Amplifier with a PMOS Lineariser," *IEEE Microwave and Wireless Components Letters*, 2020.

This paper covers the design and implementation of a high linearity CMOS power amplifier, the performance of which is tuned for higher data rates. The step-by-step procedure of achieving such a high performance of linearity is described in detail in Chapter 3.

1 Introduction

1.1 Introduction

In line with the innovations and advancements in mobile handset technology and IoT-related technologies, there is an increasing need to improve the four most important features of RF components, namely longer battery lifetime, smaller size or miniaturization, higher data rate, and lower cost. A high data rate enables more devices to transmit more information which is a difficult challenge in the IoT sector. In addition to the requirement for a high data rate, the trend towards miniaturization in IoT networks as well as smart phones and the wearable technology industry is becoming increasingly popular, as it is well documented that consumers and the technology industry require smaller, lighter electronic products with more functionality. The requirement to maximize battery life of devices in the IoT, sensor networks, the wearable technology industry, and smartphones is expected to spur the demand for ultra-low-power RF components. Furthermore, technological innovations are also sought to reduce the cost of RF components since they are critical parts of the aforementioned applications and contribute significantly to their final cost. The need for these features motivates RF component manufacturers and solution designers to focus on technological developments in their deliverables that can help meet these requirements.

For example, the first ISM transceiver chip ML5800 is produced in 2004 by Micro Linear Corporation with the focus on high data rate for streaming audio and video. It can achieve 1.5 Mbps of FSK data in the 5.725 to 5.850 GHz unlicensed ISM band. Following that, in 2008, the chip ML5805 of RF Micro Devices, Inc. is the first ISM transceiver with an integrated power amplifier. It can transmit up to 2.048Mbps. Recently, in 2020, the A5133 chip, which is produced by Amiccom Electronics Corporation, can provide longer transmission distance with higher speed of 4Mbps.

The block diagram of a simple RF transceiver module [1], presented in Figure 1-1, shows a typical RF transceiver working at UHF (450-806 MHz) frequency. Power amplifiers are the final output stage in a wireless system with the role of amplifying the RF

signal before transmitting it to an antenna [2]. Therefore, PAs and antennas are some of the most crucial parts of a wireless transceiver due to their high-power capability, their effect on the data rate and power consumption, and their large size. High linearity PAs are normally utilised to cater for high data rate requirements. In addition, various antenna design techniques have been employed to help achieve a high data rate, increase power efficiency (hence, lower power consumption) and reduce the size and cost of the RF design.

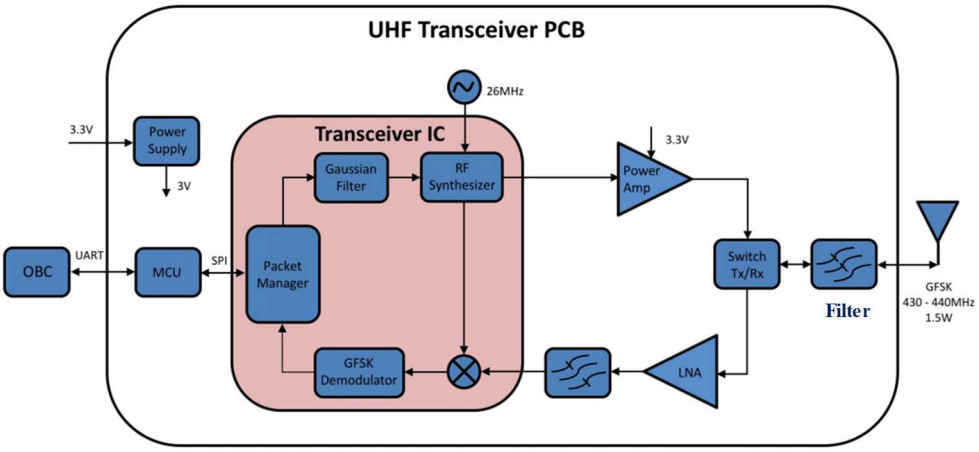


Figure 1-1. Block diagram of a typical RF Transceiver Module [1]. The PA and the low noise amplifier (LNA) are connected to the antenna through a switch and a filter.

The PA segment occupied more than 30% of the overall RF market share in 2019 and continues to increase over time due to the increased demand for 4G/5G handsets, as shown in Figure 1-2. Although there has been significant advancement in the PA industry driven by advanced technologies and companies such as Freescale Semiconductor, Texas Instruments, NXP Semiconductors, and Avago Technologies Ltd, there is still a requirement for improvement for 5G and the IoT.

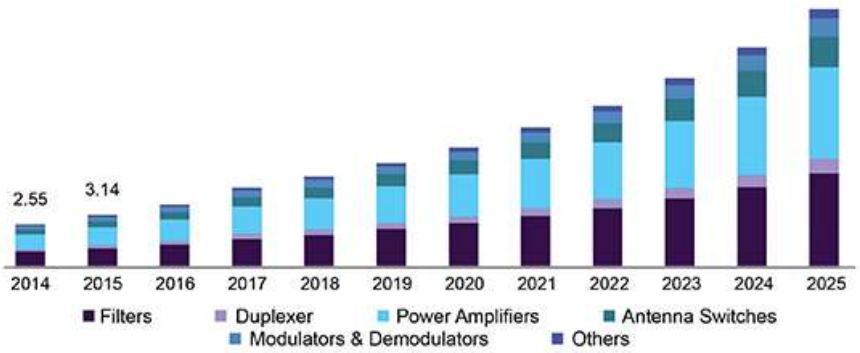


Figure 1-2. RF component market size [3]. The PA segment occupies a large portion, more than 30%, of the overall RF market share.

Specifically, since PAs are the final output stage in transmitter chains, PAs determine the overall linearity of the chains. Modulation techniques such as Code-Division Multiple

Access and (CDMA) Orthogonal Frequency-Division Multiplexing (OFDM), in which high bit-rate data are transmitted in parallel to avoid interference, have become popular because of the high demand for current high-speed wireless transmission. Because modulated high-bit rate signals have a large peak-to-average-power ratio (PARP), they can be cropped in a non-efficient transmitter PA due to its non-linearity or low dynamic range [4], lowering the effective data rate. This potential performance degradation can be avoided by having higher output power back-off (which is defined as the ratio of maximum saturation output power to lower average output power). The larger the back-off, the lower the nonlinear distortion. Therefore, recent RF PAs often need to operate in a very large linear region. On the other hand, since PAs work at a high-power range, the active components in PAs, namely parasitic gate capacitances of complementary metal-oxide-semiconductor (CMOS) transistors [5, 6] [7] and transconductance [8, 9], generate very high nonlinear components. The nonlinear components cause in-band interferences and gain compression, leading to low one dB compression points, $P_{1dB,}$ and high intermodulation distortions. For this reason, many techniques in the literature, such as adaptive bias circuit [7, 10-14], second harmonic suppression short circuit [5, 7], predistortion shunt-cold field-effect transistor (FET) [15, 16], N-type metal-oxide-semiconductor diode lineariser [17] have been applied to improve the linearity of PAs. Hence, ongoing research on high linearity PAs is needed to cater for the upcoming wireless standards which provide a very high data rate.

As shown in Figure 1-1, the antenna is connected to the PA and the low noise amplifier through a switch and a filter. Therefore, the performance of the antenna affects the whole performance of the RF transceiver in general and the performance of the PA and LNA specifically. The higher-order harmonic components should be suppressed to improve the power-added efficiency of the PA in the transmitter [18, 19]. As a result, the power consumption performance of the RF transceivers is enhanced. The suppression also helps reduce those components emitting to other communication devices. On the receiver side, harmonic suppression is required to cancel out-of-band noise and interference [20-23] to improve the data rate. Therefore, the antenna performance in harmonic suppression must be improved to achieve a better noise immunity, thus improving the data rate of communication systems. In addition, the harmonic suppression antenna helps reduce the size of the RF transceiver while improving its performance, meeting the requirement for further miniaturization. A simple and conventional approach to address these challenges is to use separated filters in series with the antenna, as shown in Figure 1-1. However, this

increases the total size, insertion loss, and implementation cost of the whole system and degrades the noise figure of the receiver. An alternative is to design an antenna that can reject unwanted out-of-band radiations and suppress higher-order harmonics. This method also achieves the miniaturization requirement of modern RF transceiver modules while improving the achievable data rate. As a result, the demand to develop harmonic suppression antennas is likely to increase in relation to future wireless devices.

Many of today's RF transceivers [24, 25] use frequency division duplexing (FDD) which requires two frequencies to carry the two simultaneous data channels, one in each direction. They are integrated extensively into cell phones and other wireless devices including the Internet of Thing devices, which by 2022, are projected to grow to a very huge number, more than the number of people in the world [26]. Given the finite availability of the spectrum and the increasing number of devices, the demand for more wireless data can only be met through an increase in spectral efficiency in wireless transceivers. In addition to well-known radio resource management techniques such as dynamic channel allocation power control, link adaptation and various diversity schemes, the in-band full-duplex operation is of great interest in relation to compact communication systems due to its capability to double the spectral efficiency [27], hence improving the data rate. Figure 1-3 in [28] shows the concept of how In-Band Full-Duplex (IBFD) operation , which allows the same frequency to be used for both receiving and transmitting, increases spectral efficiency compared to the frequency division duplex. It also shows that IBFD doubles the data rate compared to the time division duplex. Thus, the wireless capacity of IBFD is doubled compared to both the time division and frequency division duplex.

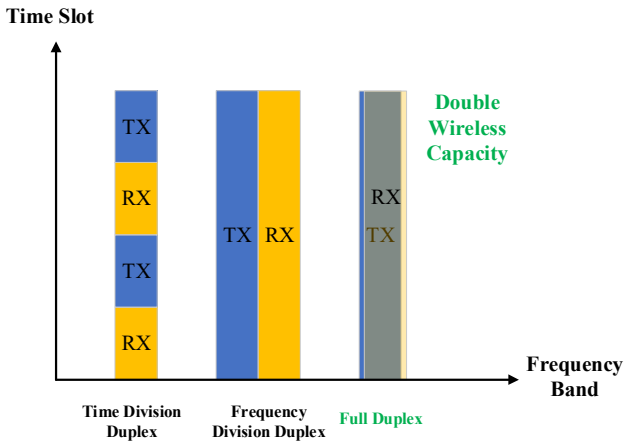


Figure 1-3. Full-duplex operation doubles wireless capacity [28].

However, the IBFD is still not widely used due to the problem of self-interference, in which radio signals from its own transmitter can be received by the receiver. Here, the power of the self-interference signal can be millions of times higher than the power of the received signal. Generally, the required amount of self-interference cancellation should be more than 100 dB [29] to completely suppress the RF leakage from its own transmitter in order to recover the actual received signals.

Therefore, many SIC techniques, such as separation and coupling networks in the antenna domain, architectures and locations in the analog domain, and channel modelling and RX beamforming in the digital domain [30] have been proposed.

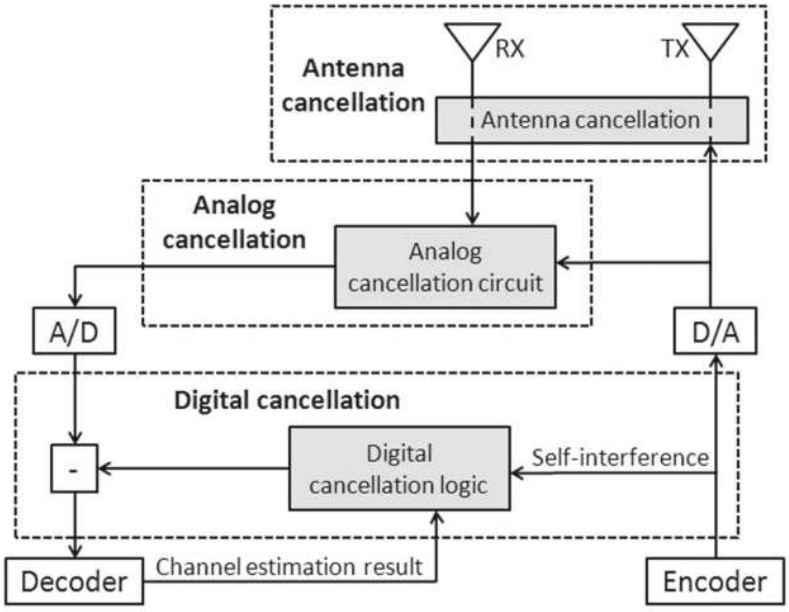


Figure 1-4. Block diagram of a typical full-duplex system [31]. The SI cancellation techniques should be implemented in all three layers of the digital, analog, and antenna domains.

These techniques must be implemented in parallel in all three layers, as shown in Figure 1-4 [31], to achieve the high 100 dB isolation between collocated TX and RX. However, most SI cancellation should be performed at the antenna stage to avoid the saturation of the radio receiver [29]. Furthermore, the passiveness of the antenna can reduce complexity in the cancelation techniques in the digital domain. Therefore, research on high isolation antennas is necessary and can be used to drive future research and accelerate the inclusion of IBFD technology within an upcoming wireless standard.

1.2 Motivations

The motivations underpinning this thesis are shown in Figure 1-5 and focus on improving the important features of RF components, namely miniaturization, high data rate,

longer battery lifetime, and lower cost of RF components. The motivations can be achieved separately by focusing on three research topics, namely high linear CMOS power amplifiers, harmonic suppression antennas, and full-duplex antennas.

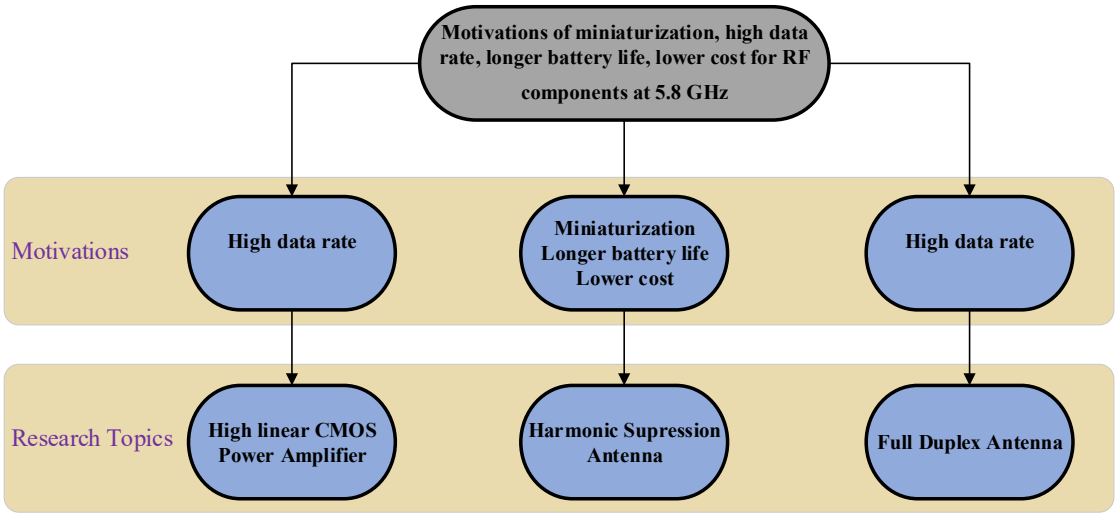


Figure 1-5. Motivations in this thesis for RF components at 5.8 GHz ISM.

1.2.1 High Linearity Power Amplifier Motivations

PA performance is heavily determined by the need for higher data rates. Figure 1-6 shows the physical data rate trend with a steady increase of typical bit rate [4] [32], from 20 Kbps of 2G standard to the 200 Mbps of the 5G LTE.

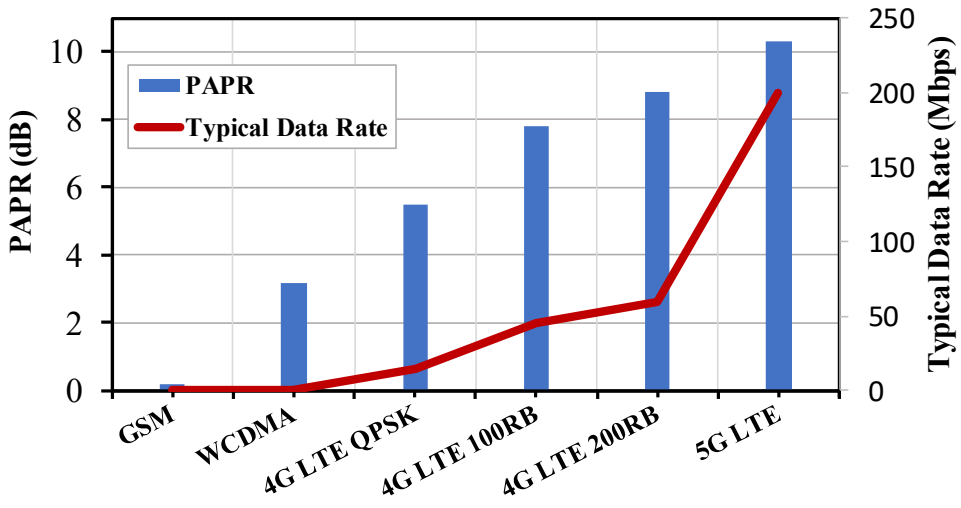


Figure 1-6. Typical data rate and peak-to-average power ratio (PAPR) for different standards of mobile communication generations [4] [32]. The data shows that the PAPR follows the same trend as the typical data rate.

Achieving a higher bit rate has a strong effect on channel bandwidth, for example, 200 kHz of 2G evolves to 100 MHz of 5G LTE. This also has a significant impact on modulation, from Gaussian Minimum Shift Keying (GMSK) modulation in 2G to 256 quadrature amplitude modulation of LTE in order to increase spectral efficiency. The increment in the complexity of modulation schemes, which aims to achieve high spectral efficiency, must also be accompanied by high PAPR modulated channels.

As described in Figure 1-6, the PAPR experienced an obvious growth, from approximately 0 dB of the 2G standard to 10.3 dB of the 5G LTE standard. Since it can be stated that at certain times, the high PAPR signals require peak power, which is much higher than the average, PAs with high linearity are necessary to avoid the clipping of the signal, leading to distortion of the transmitted signals. Therefore, the demand for higher linearity PAs is unavoidable in modern wireless communications with higher PAPR standards.

On the other hand, since PAs work at a high-power range, the active components in PAs, namely parasitic gate capacitances of CMOS transistors [5, 6] [7] and transconductance [8, 9], generate very high nonlinear distortions. Such nonlinear distortions cause in-band interferences and gain compression, leading to a low one dB compression point, $P_{1dB,}$ and high intermodulation distortions. Hence, based on the requirements of a higher data rate of upcoming wireless standards and the high internal distortions of the PAs, many techniques should be studied to improve PA linearity.

1.2.2 Harmonic Suppression Antenna Motivations

Filters are normally used in series with the antenna to suppress unwanted high-order harmonics or interference. However, the filter insertion approach fails to achieve miniaturization and often increases insertion loss and thus, leads to an increase in total implementation cost and the performance degradation of the whole system. Hence, an antenna with inherent out-of-band rejection capable of rejecting unwanted radiations and suppressing higher-order harmonics is a more cost and area efficient alternative approach.

A passive harmonic suppression antenna can be connected with an RF transceiver to reduce high harmonic components. On the transmitter side, a harmonic suppression antenna helps suppress the higher-order harmonics, which cause RF interference for other RF devices. On the receiver side, the antenna cancels out-of-band noise and interference, thus

improving the signal-to-noise ratio. More importantly, the harmonic suppression antenna can improve efficiency in active integrated antennas (AIAs).

An active antenna is an antenna that contains active electronic components such as transistors or diodes. Active antennas can play a double role as a radiating element as well as an impedance matching network, feedback network, low pass filter (LPF), and so on. Therefore, they are mostly used in situations that need a compact size such as inside portable devices. Nevertheless, active integrated antennas also require suppressing the higher-order harmonics to improve the power-added efficiency of the PA in the transmitter. In an active antenna, the antenna should suppress the higher-order harmonics to improve the PAE of the PA in the transmitter [18, 19]. On the receiver side, harmonic suppression is also required to cancel out-of-band noise and interference [20-23].

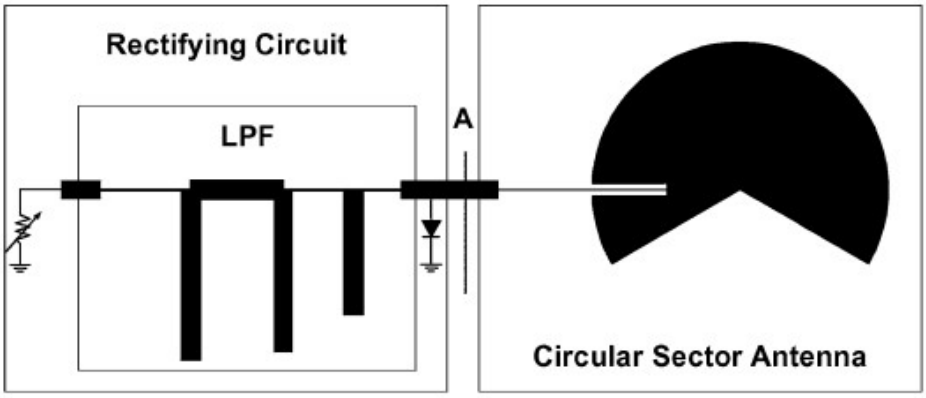


Figure 1-7. A rectifying circuit with a harmonic suppression antenna using a circular sector antenna [33]. The circular sector shape of the antenna alters the higher order resonances, shifting them away from the harmonic frequencies.

Here is an example of an AIA system, a rectenna [33], as shown in Figure 1-7, which delivers rectified RF energy into DC voltage for an overall wireless power transfer system. High efficiency is one of the most importance parameters of the rectenna. A harmonic suppression filter is normally placed between the antenna and the diode to suppress the harmonics generated by the diode, thus reducing the power loss. However, here, a circular sector antenna, which can reject the second and the third harmonics by shifting its higher order resonances away from harmonic frequencies, is implemented so that a low pass filter is eliminated. Furthermore, additional insertion loss occurring when implementing an LPW can be reduced significantly. Figure 1-8 shows that the circular sector antenna provides higher output power compared to a conventional rectangular antenna, resulting in a higher conversion efficiency.

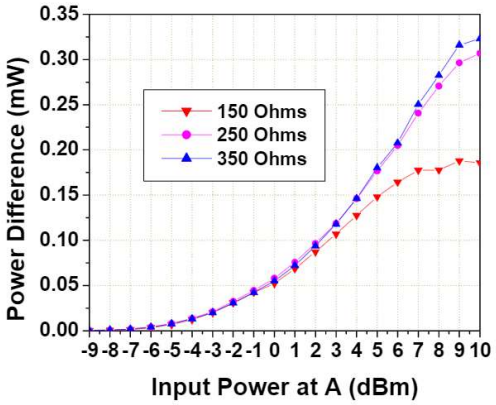


Figure 1-8. Power difference between the rectifying circuit with the circular sector antenna (harmonic suppression antenna) at 250 and 250 Ohms and the conventional rectangular antenna at 150 Ohms [33].

In another example [34], the harmonic suppression antenna, shown in Figure 1-9(b), used in an oscillator AIA, improves the free running oscillation power at 2.4 GHz to 16.2 dBm from 11.5 dBm of the conventional antenna, shown in Figure 1-9(a). The measured efficiency also increases from 9.42 % to 27.6 %.

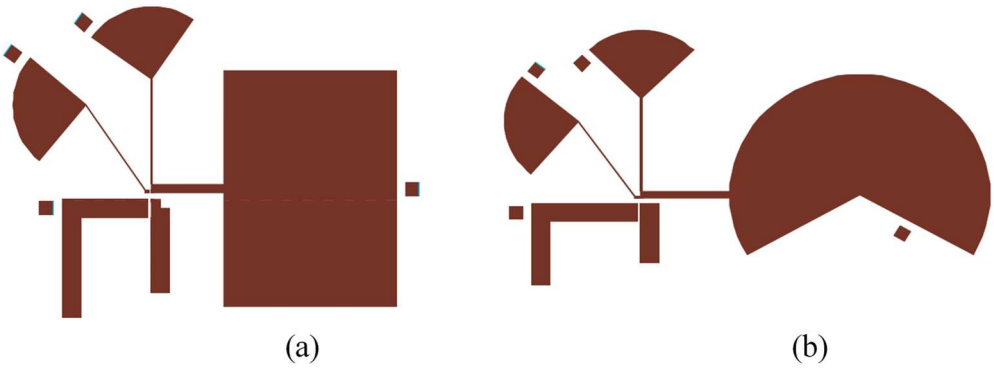


Figure 1-9. Oscillator AIA layouts with (a) conventional rectangular patch antenna (b) and circular patch antenna.

These two examples of AIAs both use the circular patch antenna for harmonic suppression, but one is a rectifier and one is an oscillator, showing that a harmonic suppression antenna can improve the output power and power efficiency in different types of active circuits. The improvement in power efficiency can lead to lower power consumption and longer battery lifetime.

As a conclusion, harmonic supersession antennas can achieve miniaturization and longer battery lifetime. In addition, the signal-to-noise ratio can be improved with this technique, leading to a higher data rate. These factors are likely to contribute to the expected growth of harmonic suppression antenna techniques in the future.

1.2.3 Full-Duplex Antenna Motivations

Current wireless devices are generally half duplex in frequency, that is, they cannot transmit or receive at the same frequencies simultaneously, which results in a big problem, namely the inefficient use of the spectral resources. In addition to various ways to increase spectral efficiency, such as dynamic channel allocation power control, link adaptation and diversity schemes, the IBFD operation has recently attracted attention. However, the biggest obstacle of full-duplex implementation is in reducing self-interference: the transmitted signal appears at its own receiver with very high power, up to 60 dB (millions) to 90 dB(billions) times stronger than a received signal, thus overwhelming the received signal. For example, a transceiver with a 0 dBm transmit power and a -90 dBm noise floor needs to cancel nearly 95 dB of self-interference to ensure the reception is not disrupted by its own transmissions.

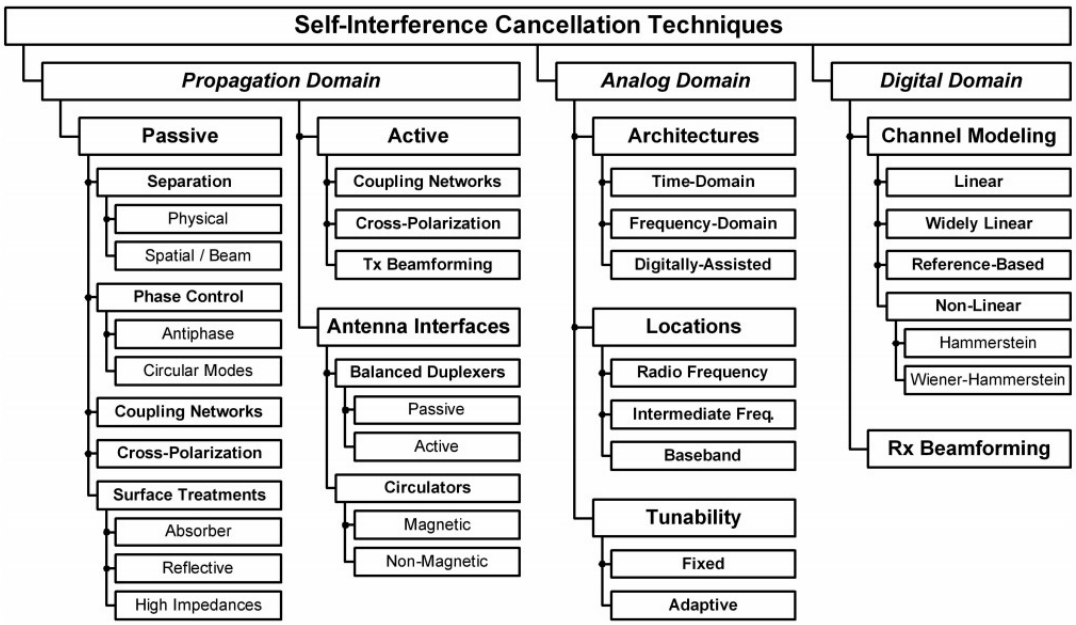


Figure 1-10. Many self-interference cancelation techniques have been proposed in the propagation, analog and digital domains [30].

As shown in Figure 1-10, many SIC techniques have been proposed in the propagation, analog and digital domains. However, recent digital and analog cancelation techniques are not sufficient to cancel self-interference. For instance, digital cancelation using a 14 bit analog-to-digital converter (ADC) can only achieve cancelation up to 54 dB [27]. Analog cancellation [35, 36] sends a cancelling signal through the second radio chain and adds it to the signal at the receiving antenna, meaning it uses knowledge of the transmitting signals to enable cancelation. This technique, which is similar to that used in a noise-cancelling headphone, can only provide about 25 dB of cancellation due to the expense of introducing numerous non-linearities and distortions to digital cancellation. Furthermore, extra RF hardware components used in analog technique such as RF combiners and RF frontends

will increase the cost significantly. Motivated by these limitations, full-duplex antenna systems, which have a very high RF isolation between the RX and TX port, have been studied extensively. For example, a single antenna with 40 dB inter-port isolation with 30 dB self-interference suppression at the digital and analog stages is deployed to implement IBFD with the required 100 dB SIC. However, if the antenna can be designed to have 70 dB isolation between the TX and RX port, 100 dB SIC can be achieved with only 30 dB SIC at the digital stage. Therefore, the transceiver can perform the IBFD operation without a duplexer and complex analog or RF domain SIC techniques.

In conclusion, the full-duplex antennas help to achieve full-duplex communication, which represents an attractive option for a high data rate by its potential to double spectral efficiency. Therefore, research on high isolation antennas is needed for upcoming wireless standards.

1.3 Research Aims

The performance of RF transceivers needs to improve to ensure high data rates, a long battery lifetime, and that they are small in size and low in cost with high reliability and yet using minimum spectrum in modern wireless communication. To meet these challenges, the designs of RF power amplifiers and antennas come into consideration. Specifically, high linear power amplifiers, harmonic suppression antennas and full-duplex antennas are motivating many studies in the RF design. This study first improves linearity or P_{1dB} in CMOS RF power amplifiers since it improves the data rate performance. Then, the rejection capacity in the out-of-band frequency range of harmonic suppression antennas is improved while maintaining a compact size and bandwidth. Finally, the isolation between TX and RX antennas in a full-duplex antenna is studied and based on this, a novel method is derived to improve it without increasing the size.

In this dissertation, all the RF CMOS power amplifiers, the three harmonic suppression antennas, and the full-duplex antenna are designed to work at 5.8 GHz. The frequency 5.8 GHz is allocated to Industrial, Scientific and Medical (ISM) radio bands and Wireless Local Area Networks 802.11a and 802.11n. In the WiFi (IEEE 802.11x standards) applications, the 5.8 GHz radio can support up to 1300 Mbps, compared to 600 Mbps of the well-known frequency 2.4 GHz [37]. Furthermore, the 5.8 GHz has less traffic than 2.4 GHz, since fewer devices work on the 5.8 GHz. Therefore, the 5.8 GHz provides much faster data connections than 2.4 GHz. In ISM applications, which can be used without a government license, there is a growth in 5.8 GHz usage especially in short-range and low-power

wireless communications. For example, in 2013, Google's Project Loon used 5.8 GHz ISM bands for balloon-to-balloon and balloon-to-ground communications [38].

In this thesis, the following aims will be accomplished:

• A novel linear cascode differential CMOS power amplifier that operates at 5.8 GHz ISM (the low-cost Taiwan Semiconductor Manufacturing Company 0.18 μm process technology is used). The P_{1dB} of the linear PA should be compared to that of its counterpart conventional power amplifier to validate the improvement. Then, a layout is created for fabrication. The layout design must be optimized to have minimum interconnect parasitics namely parasitic resistance, capacitance and inductance. The measured P_{1dB} of the whole PA should show significant improvement to be able to help with the challenges of the data rate demand. The input and output return loss should be above 10 dB and the power gain should be above 15 dB at the operating frequency of 5.8 GHz to be considered as acceptable performance. In addition to the high P_{1dB}, the PA must achieve a low quiescent current to ensure a longer battery lifetime and a small size for device miniaturization. In terms of its overall performance, the proposed PA should achieve a high figure of merit (*FOM*), which considers saturation power, gain, efficiency, and operating frequency all together.

• Two narrowband harmonic suppression antennas are developed to work for our 5.8 GHz RFID tag application with the bandwidth of 200 MHz. The radiation pattern of the radio frequency identification tag is required to be omnidirectional in order to detect the RF signal in any direction, which is suitable for the radiation pattern of a slot antenna. Based on the RFID requirement, the two narrow slot harmonic suppression antennas, a Double Slot Harmonic Suppression Antenna, and a Small Size Slot Harmonic Suppression Antenna, are proposed, both of which use the defected ground structure (DGS) technique combined with other harmonic suppression techniques. The size requirement of these antennas must be compact, (since the size of the RFID tag, and generally, IoT and wearable/portable devices are small) with the requirement of a gain larger than 0 dB. A reduction in bandwidth is acceptable in the two antennas but their modified bandwidths must still be higher than 200 MHz. However, to cater for the demand of wideband applications in IoT and wearables, a more novel slot antenna, named Wideband Triangle Slot Antenna with Out-of-Band Rejection, is proposed with strong out-of-band rejection characteristic. A much greater size reduction (in relation to its counterpart conventional antenna) compared with the size reduction of the aforementioned two antennas (also in relation to their counterpart conventional antennas) must be achieved to show a big improvement in the design technique. The proposed wideband design must realize a

significant improvement in bandwidth compared with its counterpart conventional antenna instead of exchanging bandwidth with the harmonic suppression capability.

• To address the recent demand for a high data rate for mobile, IoT, and sensor networks, a compact antenna system is designed at 5.8 GHz ISM frequency in the IBFD operation. The antenna must be designed without the use of a coupler to ensure it is small in size. The antenna should have a competitive 50 dB isolation performance while maintaining a small size and a single layer printed circuit board. The impedance bandwidth of both ports should be around 10% to show an acceptable improvement over other IBFD recent deigns. The isolation technique must be analysed using mathematical equations. Equivalent circuit models are also provided to assist the impedance optimization process.

These thesis aims are summarised in Figure 1-11 for a quick review.

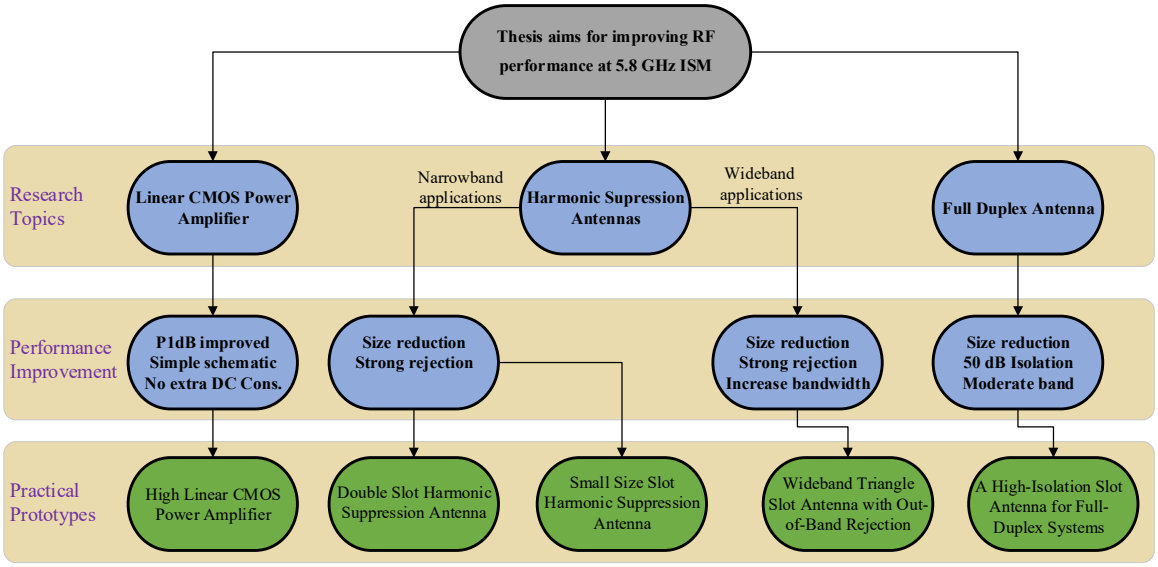


Figure 1-11. Thesis aims for improving RF transceiver performance at 5.8 GHz ISM.

1.4 Original Contribution of the Thesis

With the aim of developing a CMOS PA with improved linearity, this dissertation proposes a 5.8 GHz CMOS PA with a novel PMOS lineariser. The PMOS lineariser improves the P_{1dB} of the PA by changing the bias of the power stage when the input power reaches the input P_{1dB} point. Therefore, it can be categorised as an adaptive bias circuit. However, most of the adaptive bias circuits are based on sensing the input signals of the PA to control the PA's bias voltages. These input signals often have a small amplitude. Therefore, the adaptive bias circuits [7, 10-12, 14] often include two-stage amplifiers, envelop detectors and envelop shaping circuits, leading to high complexity, distortion due to delay through the auxiliary path, extra current consumption, and a large size. In another

improved design of the adaptive bias circuit in [13] with no additional path for detection, the circuit still consumes up to 6 mA at 1.2 V supply, which is still considerably large for an auxiliary circuit such as a lineariser. Compared to the other aforementioned adaptive circuits, the originality of this technique is in its novel idea of using both output and input signals of the PA to drive the lineariser, thus requiring only one additional bias source and almost no extra DC consumption. The mathematical model and the analysis using Kirchhoff equations are presented to show how the bias voltage is changed using the PMOS lineariser to clarify the linearity enhancement mechanism.

Next, two narrow slot harmonic suppression antennas are developed to work for the described 5.8 GHz applications with a bandwidth of 200 MHz, which is a narrow bandwidth. Based on this requirement, a Double Slot Harmonic Suppression Antenna and a Small Size Slot Harmonic Suppression Antenna are proposed. Both the narrow slot antennas use the DGS technique combined with other harmonic suppression techniques. Despite this integration, the novel proposed harmonic suppression structures reduce the length of both the antennas compared with their conventional counterpart antennas. Although the bandwidths of the proposed antennas are reduced compared to their conventional counterpart antennas due to the embedding of the harmonic suppression structures, they are still bigger than the bandwidth requirement of 200 MHz. Moreover, based on the author's knowledge, for the first time, the linear relationship between the bandwidth of the stepped-impedance-resonator slot antenna and its width is mathematically derived using transmission line model analysis and is validated using the full wave simulation of HFSS.

Then, a wideband triangle-slot antenna, named Wideband Triangle Slot Antenna with Out-of-Band Rejection, with a very high out-of-band harmonics and interference rejection is proposed while achieving a compact size. The antenna covers the whole C-band (4 GHz - 8 GHz) including the 5.8 GHz ISM and sub-6 GHz band of 5G. The antenna is developed from a rotated square slot antenna with a 50% size reduction using a small modification. Then, a DGS and thin microstrip line are embedded completely inside the main radiating slot to achieve out-of-band rejection and a reduced antenna size. Importantly, the added DGS and thin microstrip line increases bandwidth by up to 5.51 GHz (82.7% fractional bandwidth) and reduces the antenna size. The originality of this technique is in its capability to achieve wider bandwidth together with out-of-band rejection while reducing the size significantly. Furthermore, by adding matching elements using the stacked rectangular slot principle, the antenna size is reduced further, leading to a 60% reduction in size. The final

ground size is 32 x 32 mm, which is suitable for integration into portable devices. Mathematical analysis and equivalent transmission line circuit models are provided to give physical insight into the working principles of DGS and the antenna with validation from the High Frequency Electromagnetic Field Simulation Software (HFSS) simulation. The working principle of the triangle-slot antenna is explained based on the tapered slot principle and thus, helps to clarify the mechanism of how wide bandwidth is achieved using DGS and the thin microstrip line more clearly. Moreover, the return loss improvement of the matching elements is explained using the principle of the tapered slot antenna as well.

Finally, a compact slot antenna system with very high isolation between its two ports, up to 50 dB, is proposed. Unlike the previous works, a microstrip T-junction power divider, a coplanar waveguide-slotline tee, and a capacitor are used to feed the antenna instead of couplers to reduce size. At Port 1, a microstrip feeding line is coupled with a CPW-slotline tee to ensure the antenna operates in odd mode only. Port 2 uses a T- junction power divider to form a conventional array slot antenna working in even mode only. The orthogonal coupling between even mode to odd mode creates a high isolation of 30 dB. To enhance the isolation to 50 dB, one capacitor is used at the termination of the CPW to further reduce coupling between the two ports. The originality of this technique is in its capability to achieve high isolation without using a coupler, thus achieving a compact size. To clarify the principle of the isolation, the coupling between two ports is investigated extensively using even and odd mode analysis and the three port S-parameters method. In addition to the isolation, the impedance of the two ports are analysed in detail using equivalent transmission line circuit models in even mode and odd mode with validation from the HFSS simulation, thus assisting the impedance optimization process. To the author's best knowledge, this is the first time a high isolation IBFD antenna is analysed extensively with a mathematical model.

1.5 Significance of the Research

The original contributions of this thesis lead to many theoretical and practical benefits for CMOS power amplifiers, harmonic suppression antennas, and full-duplex antennas.

First, the PA achieves a competitive performance with the lowest DC quiescent current, small chip size and moderate P_{1dB} at the highest frequency and the lowest supply voltage compared to the existing works in [15, 39, 40]. The quiescent current is 44 mA, while those of [15, 39, 40] are 95 mA, 156 mA, and 639 mA respectively. The P_{1dB} of the linear PA improves as much as 2.6 dB compared to its counterpart conventional power amplifier in the simulation. With low voltage 1.8 V supply, the linear PA delivers a measured PAE of

22.5% and a measured P_{1dB} of 17.5 dBm at 5.8 GHz carrier frequency with a chip size of 1.07 mm^2. Furthermore, the proposed PA has noise immunity due to its differential structure, which is not available in the single-ended structure. The detailed mathematical analysis provided will significantly help designers understand and adjust the parameters and factors of the PMOS lineariser, which have the highest and lowest sensitivity in the output power of a PA circuit.

Next, the two narrowband antennas, the Double Slot Harmonic Suppression Antenna and the Small Size Slot Harmonic Suppression Antenna, are proposed at the 5.8 GHz ISM, all using the DGS technique combined with other harmonic suppression techniques. The two antennas have a narrow impedance bandwidth of less than 10%, suitable for narrow bandwidth applications. The narrow bandwidth also allows the width of the both the antennas small since the bandwidth and width are in a linear relationship. The gains of the two antennas are around 0 dB, which meet the specifications of most 5G, IoT and wearable applications. The omnidirectional radiation patterns of both antennas can detect RF signals at any angle. The linear relationship between the bandwidth of the stepped-impedance-resonator (SIR) slot antenna and its width is mathematically derived for the first time using transmission line model analysis and validated using the full wave simulation of HFSS, which helps other antenna designers to choose a balance between harmonic suppression capability and bandwidth performance. The measured |S11| within the rejection band remains larger than 2 dB from 6.5 GHz to 20 GHz, showing very competitive out-of-band rejection with respect to the previously designed antennas.

Then, a wideband antenna, named Wideband Triangle Slot Antenna with Out-of-Band Rejection, covers the whole C-band (4 GHz - 8 GHz) including the 5.8 GHz ISM and sub-6 GHz band of 5G (the next generation of mobile broadband after 4G LTE connection) is introduced. The antenna has the final ground size of 32 x 32 mm^2, which is suitable to be integrated into portable devices. The antenna uses a single layer substrate, achieving a low cost in mass production. The mathematical analysis helps designers understand and adjust many parameters and factors of the triangular slot antenna, which have the highest and lowest sensitivity in the impedance of the antenna. Mathematical analysis and equivalent transmission line circuit models are provided to give physical insight into the working principles of DGS. The proposed antenna has the widest FBW and the largest realized gain among the previously designed antennas. The |S11| within the rejection band remains larger than 1.2 dB up to 26.5 GHz showing the highest out-of-band rejection with respect to the previously designed antennas. The proposed antenna has the second-smallest ground size among the recent designs of harmonic suppression antennas. The proposed antenna offers

a 60% size reduction in the main radiating slot, compared with the rotated square slot antenna operating at the same frequency. Overall, the designed antenna achieves a highly competitive performance in comparison with the state-of-the-art harmonic suppressed antennas in the literature.

Third, a single-layered slot antenna system working at 5.8 GHz ISM frequency is proposed for IBFD applications. The design has omnidirectional radiation patterns at both ports, which is highly desirable in WLAN systems. The proposed antenna can also be deployed as a dual-polarized antenna. The antenna uses a single layer which significantly reduces the fabrication cost in mass production. Since the antenna has two ports with two modes, some parameters and factors affect the impedance of only one port, whereas others affect both ports, thus complicating the impedance optimization process. Therefore, mathematical analysis and equivalent transmission line circuit models in even mode and odd mode are provided to give physical insight into the working principles of the antenna with validation from the HFSS simulation, thus easing the impedance optimization process. To the best of our knowledge, none of the existing works on full-duplex antennas provide equivalent transmission line models for impedance and isolation optimization. The proposed antenna shows higher isolation, 50 dB, than the two similar designs, the CPW antenna with 30dB [41] and array monopole 35 dB [42], while its bandwidth is the second compared to the bandwidth reported in [41]. Overall, the proposed antenna has the highest isolation and the second-best size compared to the recent full-duplex antennas [42-46], but with a single layer PCB.

Lastly, the comprehensive literature review undertaken in this study can be used as an independent systematic review of recent linearity techniques, out-of-band rejection techniques, and isolation techniques to help understand all the advantages and disadvantages of the available techniques in various aspects of power amplifiers and antennas at the circuit level.

1.6 Research Methodologies and Techniques

This section presents the specific methods used in this thesis to realize the research aims detailed in section 1.3.

Firstly, an exhaustive literature review was conducted so that a list of the current challenges, pressing demands, current solutions and their shortcomings could be identified. However, it was necessary to cross the border of a specific area to a larger range of applications. Linearity in the CMOS Power Amplifier is application-specific and therefore is as extensive as integrated circuit applications. They can be applied to a low noise

amplifier (LNA) or a voltage-controlled oscillator and vice versa. Out-of-band rejection techniques in the microstrip antenna are, in some points, similar to the microstrip filter, so the techniques in the filter can be applied to the antenna and vice versa. High isolation techniques can be found not only in the antenna, but in the band-stop filter as well. As a result, to identify the challenging issues, it is necessary to study all the related techniques in different fields, compare the outcomes of the research with previous studies, position the remaining problems and finally select the most prevalent challenging problems and current solutions.

These available solutions were simulated with the current CMOS circuit topology and antennas and the results were carefully analysed. The CMOS power amplifier design used the 180nm interoperable Process Design Kit (iPDK) support by TSMC using Electronic Design Automation (EDA) tools from Synopsys for modelling and simulation. The microstrip transformers or balun in the PA were simulated using a 3D electromagnetic simulator, Ansoft HFSS. The rejection and full-duplex antennas also require simulation in HFSS. In parallel, the physical analysis of the circuits' behaviour together with mathematical analysis studying numerous design techniques in the previous literature helped in proposing new techniques.

Based on the current challenges in the industry, the demands of consumers and the future trajectory of IoT, and wearable and portable devices, numerical specifications were set for each of CMOS PAs, harmonic suppression antennas and the full-duplex antennas whenever a solution was proposed. The specifications must cater for the requirements as mentioned above and improve the previous relevant measurement results in the literature. The P_{1dB} of the CMOS Power Amplifier should be comparable with the recent designs of PAs using the same technology, as discussed earlier. The operating bandwidth of both the rejection antenna and the full-duplex antenna should be comparable or better with recent designs to address the data-rate challenges. The return loss in the rejection range of the rejection antenna should be comparable or better than the other antennas in the same fields, while the isolation of the full-duplex antenna should be comparable or better than the isolation of other recent antennas to validate the improvement of the proposed techniques. The simulation results were compared with these required specifications to know where the optimization process needs to be stopped.

After achieving satisfying results by means of simulating the techniques which are applied on the CMOS power amplifier and antennas, the next step was collecting the measured results by preparing the prototypes. The detail of the methodology of the PA is

given in Chapter 3 while details of the harmonic suppression antenna and full-duplex antenna are given in Chapter 4 and Chapter 5, respectively.

Finally, the prototype of the PA circuit used the low cost commercial TSMC 180nm interoperable Process Design Kit (iPDK) with 1 poly-6 metal layer, 20 KÅ Ultra Thick Metal (UTM) and 2fF/μm2 Metal-Insulator-Metal (MIM). The prototype was fabricated and packaged by Europractice company for physical characterisation and verification. The antennas were designed and implemented using high frequency materials, namely Taconic TLY-5 and Roger Duroid 5880, and measured using network analysers and anechoic chambers to verify the results under ideal environments. If the measured results of the PA and antennas did not match with simulation results, the root causes were analysed, and new solutions were proposed. Then, the prototypes were fabricated again to confirm the analyses.

1.7 Thesis Organisation

The introduction chapter began with explaining the motivation to improve the performance of the RF components in RF transceivers, which are miniaturization, high data rate, longer battery lifetime, and lower cost. Then, the consequences of this growth in CMOS power amplifiers, out-of-band rejection antennas and full-duplex antennas were explored. Based on these challenges, the thesis goals and originality were stated in detail after which the methodology used to achieve these goals was reported.

The literature review in Chapter 2 starts with a brief introduction of its outline. Next is the literature review on CMOS PAs, focused on some well-known linearity techniques including adaptive bias and second harmonic short circuit. Then, a comprehensive literature review is presented on out-of-band rejection antennas, especially in relation to particular techniques such as the Defected Ground Structure (DGS), stepped structure, thin microstrip line and metal-to-metal (MIM) cap. Finally, a literature review is conducted on full-duplex antennas, especially on coupler, coplanar waveguide configuration, and reflective termination.

Chapter 3 explains how the CMOS RF power amplifier is designed. First, the basic parameters of a RF power amplifier are introduced. Then, a description of the design techniques with a two-stage differential amplifier and matching networks follows. The schematic, layout, and bond-wire diagram of the proposed power amplifier are shown. Next, the implementation prototype and the results are detailed with a comparison to the simulation. Finally, the comparison of the PA performance with other designs of PAs in literature is presented.

Chapter 4 details how the three harmonic suppression antennas are designed. First, the basic parameters of an antenna are introduced. Then, the design process of two narrowband antennas and a wideband slot antenna, all with out-of-band rejection is described. The results are presented and compared with the simulation results. Finally, the performance of the wideband antenna with other recent harmonic suppression antennas is compared.

Chapter 5 focuses on how a full-duplex antenna is designed. First, an isolation investigation is carried out. Then, equivalent circuits with a parameter study are conducted to help other researchers understand the working principle of the antenna. After this, the results are described and compared with the simulation results. Finally, the antenna performance is compared with other recent antennas.

Chapter 6 summarizes the challenges, methodologies, and achievements. It also offers detailed suggestions for future works and opportunities as a result of this research.

2 Literature Review

2.1 Introduction

This chapter reviews the existing work to provide the background knowledge and working principles of the reviewed techniques.

Section 2.2 presents the available techniques in RF CMOS PAs, which improve linearity at the different design levels of abstraction with their respective advantages and disadvantages that lead to the proposed technique utilised in this thesis. The two most popular linearity techniques, namely adaptive bias and second harmonic short circuit, are reviewed because they focus on improving one dB compression point, P_{1dB}, which is the most popular linearity parameter because it defines the maximum output power of an RF power amplifier.

This is followed by a description of the out-of-band rejection techniques for antennas in section 2.3. The reviewed harmonic suppression techniques include defected ground structure, stepped slot, thin microstrip line, and metal-insulator-metal cap. All these techniques have the capability to suppress harmonic frequencies with the potential of maintaining or reducing the size of the main radiating element. These techniques can be combined, leading to new harmonic suppression techniques resulting in superior performance. These new techniques are applied in all three of the harmonic suppression antenna designs.

The isolation techniques of the full-duplex antenna systems are discussed in section 2.4. The three presented techniques are coupler, coplanar waveguide configuration, and reflective termination. The coupler and coplanar waveguide configuration techniques are extensively studied in the literature whereas the reflective termination has recently emerged as a potential candidate due to the small increment in size. The reflective termination technique can be combined with the coplanar waveguide configuration technique to achieve a very high isolation, which is proposed in chapter 5.

All the aforementioned techniques have their own existing issues. Thus, mitigating solutions are needed and are discussed briefly in section 2.5.

2.2 CMOS Power Amplifier with Linearity Techniques

Due to high demand for high-speed wireless transmission, modulation techniques such as CDMA and OFDM, in which high bit-rate data are transmitted in parallel to avoid interference, have become popular. These modulations require the high linearity performance of RF transceivers. Therefore, several techniques have been proposed to improve the linearity of PAs. Some of the most popular linearization techniques are considered to linearize the PA, such as adaptive bias circuit [7, 10-14], second harmonic short circuit [5, 7], capacitance compensation [6], predistortion shunt-cold FET [15, 16], NMOS diode lineariser [17], multiple-gated transistor (MGTR) [8, 47], and active feedback lineariser (AFL) [48]. Table 2-1 compares the most prominent advantages and disadvantages of these techniques.

Table 2-1. Comparison of different techniques

References	Linearity Techniques	Main Novelty	Pros	Cons
[7, 10-14]	Adaptive bias circuit	Bias voltage follows input power level, thus compensate for the gain compression at P_{1dB} point	Improve P_{1dB} effectively	Does not improve IMD Extra DC power consumption Complex and large circuit
[5, 7]	Second harmonic short circuit	Eliminates the second harmonic voltage	Improves IMD and P_{1dB} Uses only passive caps	Needs large space due to large value of MIM caps
[6] [48]	Capacitance compensation	Compensates the nonlinear gate-source capacitance of a NMOS device	Improves ACPR and IMD3	Lower gain Does not improve P_{1dB}
[15, 16]	Predistortion shunt-cold FET	Introduces a constant loss at low power range and reduces the loss at a high-power range	Improves P_{1dB}	High insertion losses at low input power Extra two bias voltages
[17]	NMOS diode lineariser	The diode can maintain the gate bias voltage level at high input power	Improves P_{1dB} and ACPR Small size	The improvement in P_{1dB} is limited
[8, 47]	Multiple-gated transistor (MGTR)	Transconductance cancellation mechanism	Improves IMD and P_{1dB}	Needs high precision of nonlinear cancellation Extra size of auxiliary circuit
[48]	Active feedback lineariser	Maintains a constant feedback resistance at low input power and increases feedback resistance at high input power	Improves P_{1dB}	Has little effect on AM–PM distortion

Of these, the adaptive bias technique is well known for improving linearity efficiently, especially P_{1dB}, because it changes the working class of power amplifiers. In this technique, the gate bias voltage is driven based on the input or output power levels. The P_{1dB} point will be boosted near the saturation power level. However, most of the adaptive circuits use the input signals of PAs, which are small, to control the bias voltages of PA. Therefore, the

adaptive bias circuits must use at least two amplifier stages to provide enough gain, leading to the design's complexity, extra current consumption and bigger size. For example, the two-diode adaptive bias circuit in [13] consumes a current of up to 6 mA, which is considerably large for a lineariser. The second harmonic short circuit is extensively deployed in the literature because it can be combined with other linear techniques such as adaptive bias circuit. The only drawback of this technique [5, 7] is that the MIM cap value is normally large in order to suppress the second harmonic. In the capacitance compensation technique in [6] [48] , a PMOS transistor is placed alongside a NMOS device in order to compensate the gate-source capacitance of the NMOS transistor. The total capacitance seen at the NMOS gate will be a constant, which reduces the distortion generated by the NMOS gate source capacitor. However, the technique only improves ACPR and IMD3, not the P_{1dB}, in exchange of some dB loss in gain due to the increased capacitance. The predistortion shunt cold-FET technique is utilized to improve P_{1dB} by introducing a constant loss at a low power range and reducing the loss at high power range; thus, achieving a gain expansion characteristic [15, 16]. Nevertheless, the shunt cold-FET introduces high insertion losses, decreasing around 2 dB of gain of the PA, at low input power due to the large gate width and requires two additional bias sources. The NMOS diode lineariser technique also improves linearity with a simple circuit and small size as the diode can maintain the gate bias level at high input power [17]. However, it does not change the class of PA at high power, thus the improvement in P_{1dB} is limited. The diode techniques can be used in output matching to improve linearity characteristics [49]. Nevertheless, there is no improvement in P_{1dB} but in intermodulation (IMD) only. The multiple-gated transistor (MGTR) technique, which employs the transconductance cancellation mechanism, requires high precision of nonlinear cancellation between the main and auxiliary paths and thus, has a higher design complexity [8, 47]. Furthermore, the auxiliary transistors are a considerable size compared to the main transistors, which in turn increases the total size of the PA. The active feedback lineariser technique can improve linearity by maintaining constant feedback resistance at low input power and increasing feedback resistance at high input power hence, achieving a gain expansion [48].

However, in this section, the two most well-known linearity techniques, namely the adaptive bias and the second harmonic short circuit techniques, are reviewed in detail because they are effective in improving one dB compression point, P_{1dB}, which is the most popular linearity parameter.

2.2.1 Basic Parameters

This section briefly details the three most important parameters of a CMOS PA, namely $P_{1dB,}$ power-added efficiency (PAE), and Rowlett stability factor K. Other parameters such as gain, output power, and impedance matching are also important, but not specific for a power amplifier and hence, are not mentioned here for brevity.

There are several methods to measure the nonlinearity of a PA which can be characterized by output power 1dB (P_{1dB}) compression point, 3rd order Intermodulation Distortion, 3rd order Intercept Point Adjacent Channel Power, Multi-Tone Power Ratio, and Error Vector Magnitude. This thesis focuses on improving linearity in one dB compression point P_{1dB} because it is the most useful linearity parameter. Once an amplifier reaches its $P_{1dB,}$ it goes into compression and becomes a non-linear device, producing distortion, harmonics and intermodulation products. Amplifiers should always be operated below the compression point. Moreover, P_{1dB} can be measured easily using a spectrum analyser.

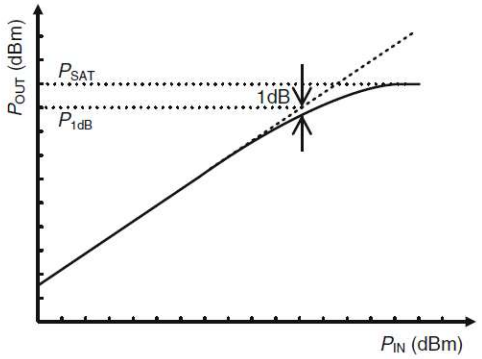


Figure 2-1. Definition of P_{1dB} [4]. The P_{1dB} is the output power value at which the power gain drops one dB from its constant value.

Figure 2-1 illustrates the input/output power curve of a PA in dBm, including the output power one dB compression point, $P_{1dB,}$ and the saturation output power, P_{SAT}. These are two of the fundamental parameters representing the linearity performance of a PA. The P_{1dB} is the output power value at which the power gain, which is equal to P_{OUT}-P_{IN}, drops 1 dB from its constant value. Once a PA reaches its P_{1dB} point, it begins to work in the compression region. Above this point, its harmonics and intermodulation distortions become more significant. Therefore, the PAs should be designed so their output power levels, which are defined in many communication standards, are well below the compression points.

The P_{SAT}, shown in Figure 2-1, is the maximum output power that a PA can reach where the PA suffers heavily from distortion. At this point, the gain is much lower than its constant value.

The power-added efficiency (PAE) [50] is defined as the ratio between the RF power added to the PA and the DC power consumed in order to get this addition. It is described as follows:

$$PAE = 100\ X\ \frac{P_{OUT} - P_{IN}}{P_{DC}} \tag{2.1}$$

A practical and common parameter, the Rowlett stability factor, K, [50] is used to check the stability condition in a small signal, which is expressed as follows:

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{2.2}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

where S_{11}, S_{22}, S_{21}, and S_{22} are the S-parameters of an amplifier with two ports. When K>1, it means that the amplifier has an unconditional stability.

However, the K factor can only check the stability condition at a small signal condition since most commercially available network analysers can only measure the small signal S-parameters. Second, the K factor cannot be applied for multistage PAs. Therefore, spectrum analysers and signal source analysers are often used in addition to the K-factor to check if there any oscillations, noise bumps or spurs come out of the PAs.

2.2.2 Adaptive Bias

The works in [7, 10-14] demonstrate that the adaptive bias control technique can improve both the linearity and efficiency in PAs. This technique drives the gate bias voltage based on the input or output power levels. When a high voltage signal enters the PA, the gate bias voltage is driven from low to high (close to Class A). As known, after the PA reaches P_{1dB}, the gain will be degraded quickly. However, the adaptive bias will increase the power gain in order to compensate the gain reduction. The P_{1dB} point will be boosted near the saturation power level. Therefore, this technique minimises the power back-off (difference between the peak power level and the P_{1dB} power level) from the peak.

A highly efficient linear power amplifier with an adaptive bias control circuit is proposed in [51]. The linear PA is biased adaptively following to its input power level to efficiently enhance output power. The block diagram, shown in Figure 2-2, in [13] represents the power amplifier with the adaptive circuit in [51].

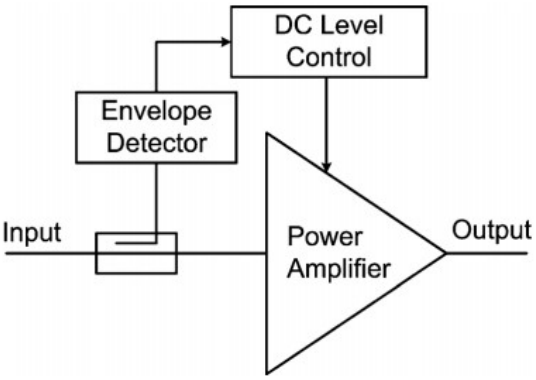


Figure 2-2. A typical adaptive bias block diagram [13]. The envelope detector senses the strength of the input signal and the DC level control converts the signal level into a proper DC bias of the power amplifier.

Since the input power is small, the adaptive bias circuit, shown in Figure 2-3, must be designed with several amplifiers to achieve enough output power to drive the bias voltages of the power amplifier.

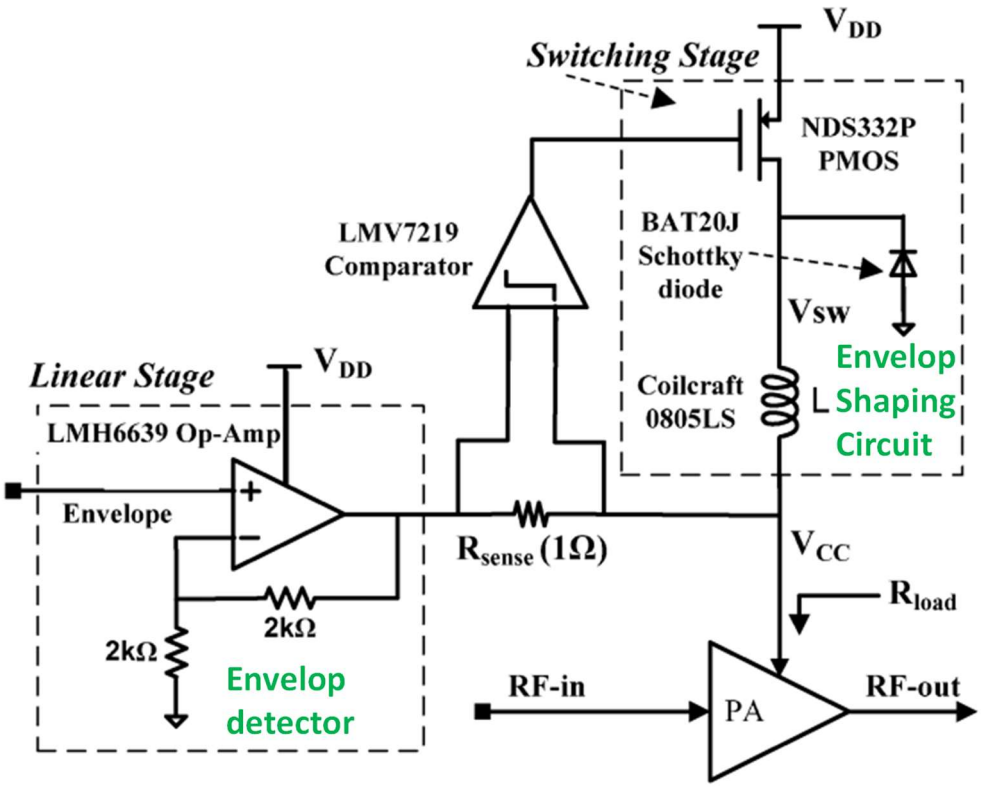


Figure 2-3. Circuit diagram for the adaptive gate bias circuit [51]. The circuit is complicated with several operational amplifiers, attenuator, and Schottky diodes. The quality of the graph is low due to the source file.

The gate voltages of the power amplifier, shown in Figure 2-4, have been controlled by the shapes which have been generated by the circuit in [52].

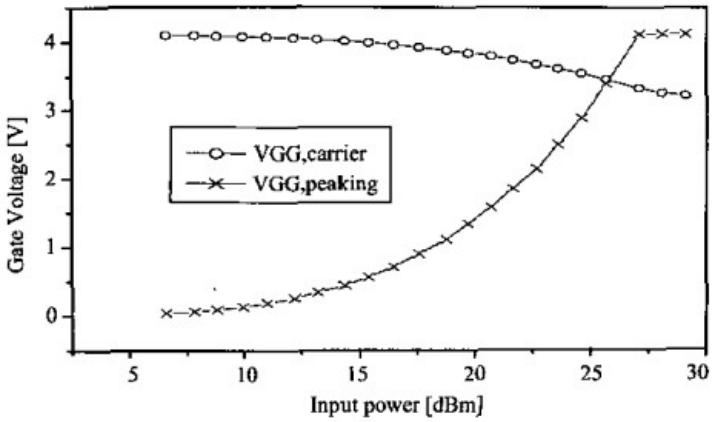


Figure 2-4. Control shapes of the two gate voltages for the adaptively controlled power amplifier [52]. The graph shows that the gate voltage of the peaking amplifier increases adaptively with the input power. The quality of the graph is low due to the source file.

The output power improves 2.2 dB and 1.4 dB compared to the two counterpart amplifiers which are class AB and Doherty amplifiers. In addition to linearity, the efficiency of the proposed amplifier is significantly enhanced. The efficiency of the amplifier is improved by 41 %, which represents a 16.5 % and 12.9 % improvement compared to the class AB and Doherty amplifiers, respectively. However, the enhancement in efficiency and linearity comes at the price of an additional large and complex adaptive circuit.

In an Enhanced Data for Global Evolution/Global System for Mobile (EDGE/GSM) Quad-Band CMOS Power Amplifier design [13], an adaptive bias circuit is proposed to boost bias voltages at large input signals to increase P_{1dB} close to the peak power. Compared with the conventional adaptive bias scheme in Figure 2-2, the proposed adaptive bias scheme, shown in Figure 2-5, has no additional path for detection and conversion from RF signal into dc bias. Thus, the circuit is simpler and easier to design and implement.

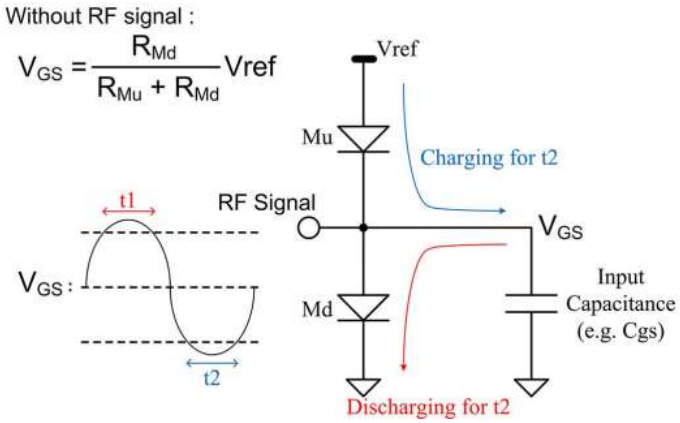


Figure 2-5. The proposed adaptive bias scheme [13]. When the RF input signal grows large enough to turn on and off the diode Mu and Md, the proposed adaptive bias circuit begins its operation in a similar manner to a charge pump in a phase-locked loop (PLL).

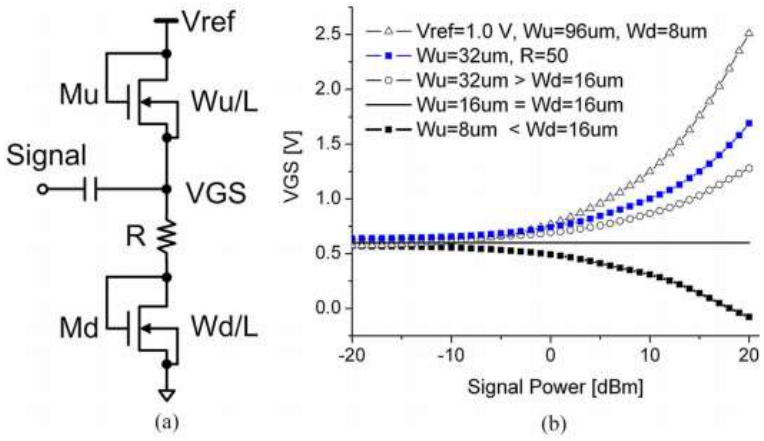


Figure 2-6. (a) The circuit design based on the scheme in Figure 2-5. (b) The simulation results of VGS with different sizes of the Mu and Md diodes. The graph shows the bias voltage VGS follows adaptively with the signal power, i.e. input power.

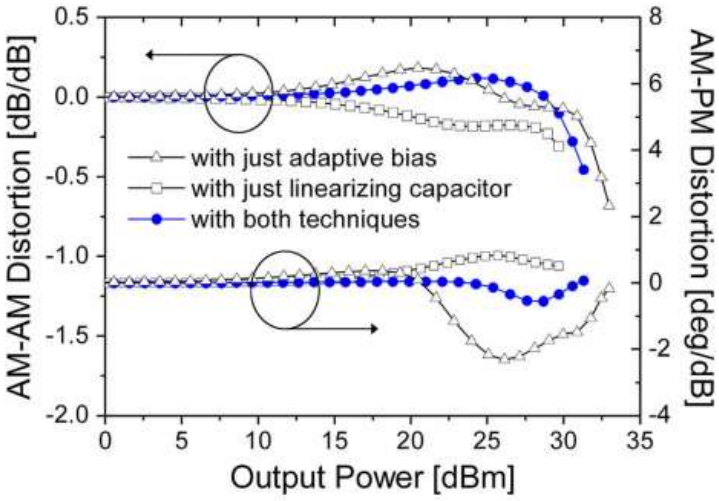


Figure 2-7. Calculated AM-AM and AM-PM distortions. The adaptive bias technique is combined with the linearizing capacitor technique to improve both AM-AM and AM-PM distortions. The adaptive bias technique alone can provide remarkable improvement in AM-AM distortions.

Figure 2-7 shows the simulated amplitude modulation-amplitude modulation (AM-AM) and amplitude modulation-phase modulation (AM-PM) distortions versus output power. The adaptive bias technique alone can provide remarkable improvement in AM-AM distortions. The proposed PA shows a very competitive performance of 34.5 dBm output power and 55% PAE in GSM mode. However, since the size of the Mu and Md transistors is large (32um and 16um, respectively), the DC current consumption of the adaptive bias circuit is around 6 mA, which cannot be ignored if the technique is applied in lower power designs.

In another example of a 2.4 GHz Doherty power amplifier [14], a small fraction of the input power is extracted from the auxiliary input, as seen in Figure 2-8. The adaptive bias circuit comprises an envelope detector stage, which includes a diode and low pass filter

circuit, and a DC level control or envelop shaping circuit. The block diagram of this circuit is similar to that of Figure 2-2 and Figure 2-3.

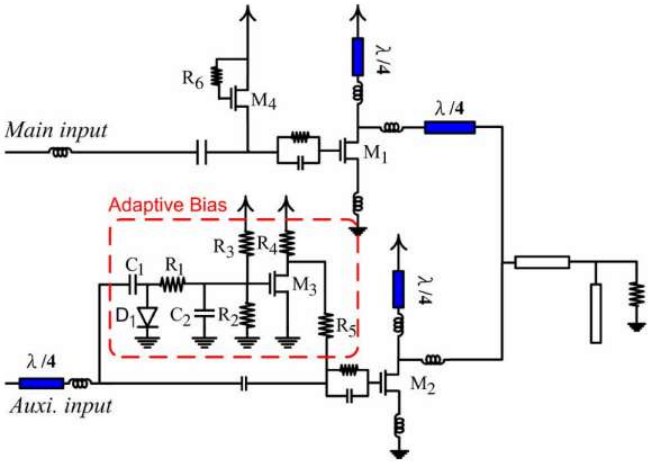


Figure 2-8. A 2.4 GHz Doherty power amplifier (PA) with adaptive bias control circuit [14]. The adaptive bias circuit detects the RF signal extracted from the auxiliary input power.

When the input driving levels are low, the magnitude of the negative DC voltages after the low-pass filter (R_1-C_2) is so small that the auxiliary power device M_2 is not turned on because of a low drain voltage of M_3. As the input driving level is high, the negative DC voltage after the low-pass filter will pull down the voltage at the gate of M_3, leading to the drain current of M_3 being decreased and the drain voltage of M_3 being increased. It can be said that the bias voltage of the auxiliary power device will follow with the input power adaptively, as seen in Figure 2-9. As a result, the measured P_{1dB} can reach up to 21.4 dBm with this technique. Furthermore, the PAE degradation due to 6-dB backoff from of P_{1dB} this work is 36%, which is the best of the CMOS RF PAs compared to the previous literature.

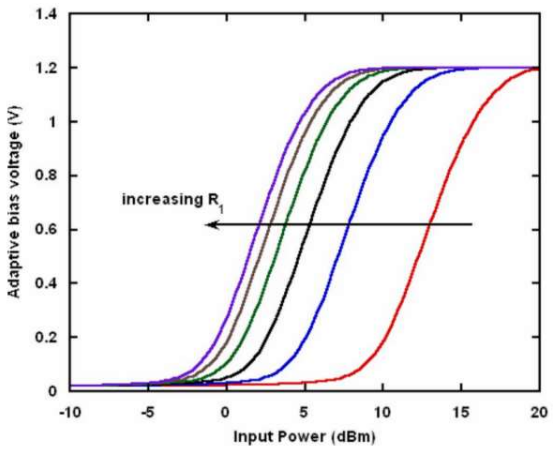


Figure 2-9. Curve of adaptive bias voltage in respect to input power. The bias voltage increases adaptively with input power.

In conclusion, the adaptive bias technique can extend P_{1dB} to ~1 to 3 dB compared to the conventional counterpart PAs. Furthermore, it can improve efficiency in some cases. The adaptive bias circuits normally are complex and occupy a large area, thus increasing cost, design time, and size. Here, the size increment does not comply with the current trending of miniaturization. The adaptive bias circuits also consume a considerable dc power. This can lead to the degradation of battery lifetime, which is not acceptable in modern RF transceiver designs with the demand of a longer operating time.

2.2.3 Second Harmonic Short Circuit

The works in [5, 7] demonstrate that the second harmonic suppression short circuit technique, including the second and the third harmonic components, can boost both the linearity and efficiency in PAs. When using the second harmonic control circuit at the input,

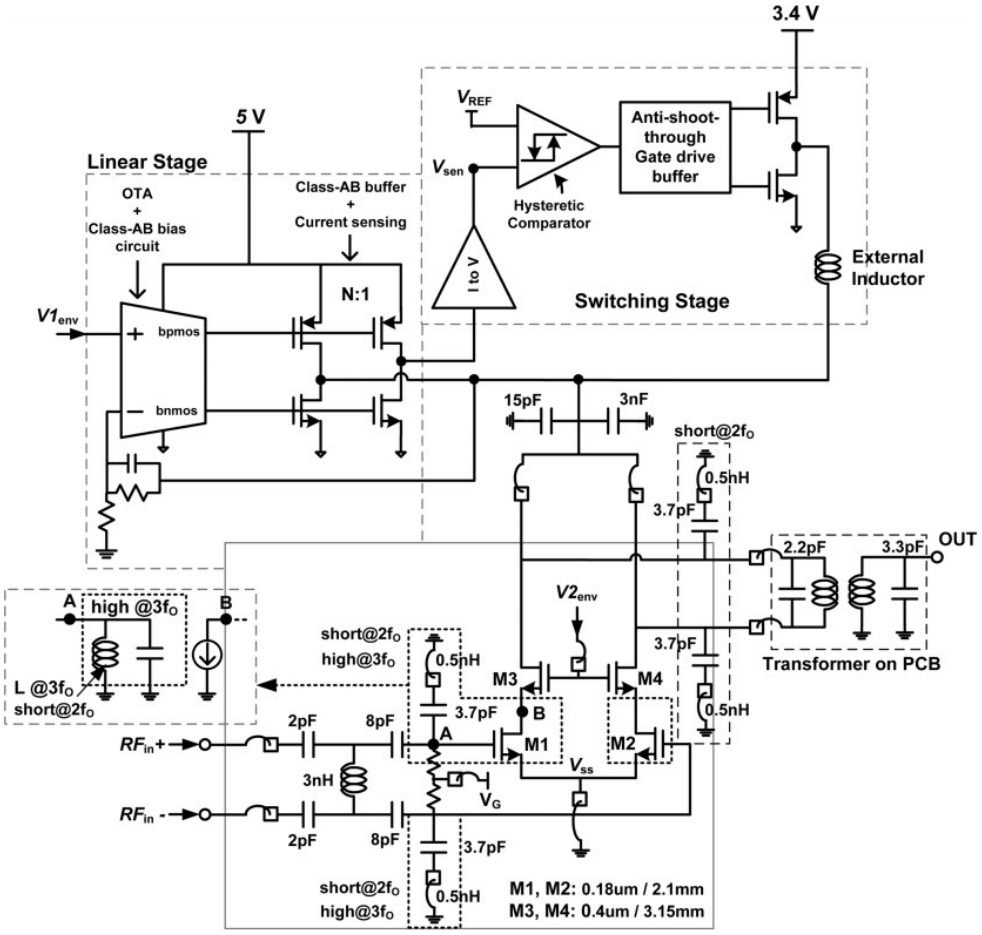


Figure 2-10. Schematic of the envelope tracking CMOS PA with the supply modulator [5]. The second harmonic short circuits are placed at the input and output of the PA.

the circuit will compensate for the distorted input signal generated by the parasitic capacitances of the transistors, resulting in a more linear operation. On the other hand, the

second harmonic short circuit at the output eliminates the second harmonic voltage, thereby reducing the up-conversion of the component to the third-order intermodulation distortion capacitances of the transistors, resulting in a more linear operation. On the other hand, the second harmonic short circuit at the output eliminates the second harmonic voltage, thereby reducing the up-conversion of the component to the third-order intermodulation distortion (IMD3) and fifth-order intermodulation distortion (IMD5) thus, improving the efficiency of the devices. The third harmonic trap, which is also a short circuit, will also improve linearity by reducing the third harmonic. However, the effect is smaller than that of the second harmonic control circuit because the third harmonic is significantly lower than the second harmonic component in general.

As seen in Figure 2-10[5], the second harmonic short circuits are placed at the input and output of the PA. The capacitance between the gate and source of the transistor is not

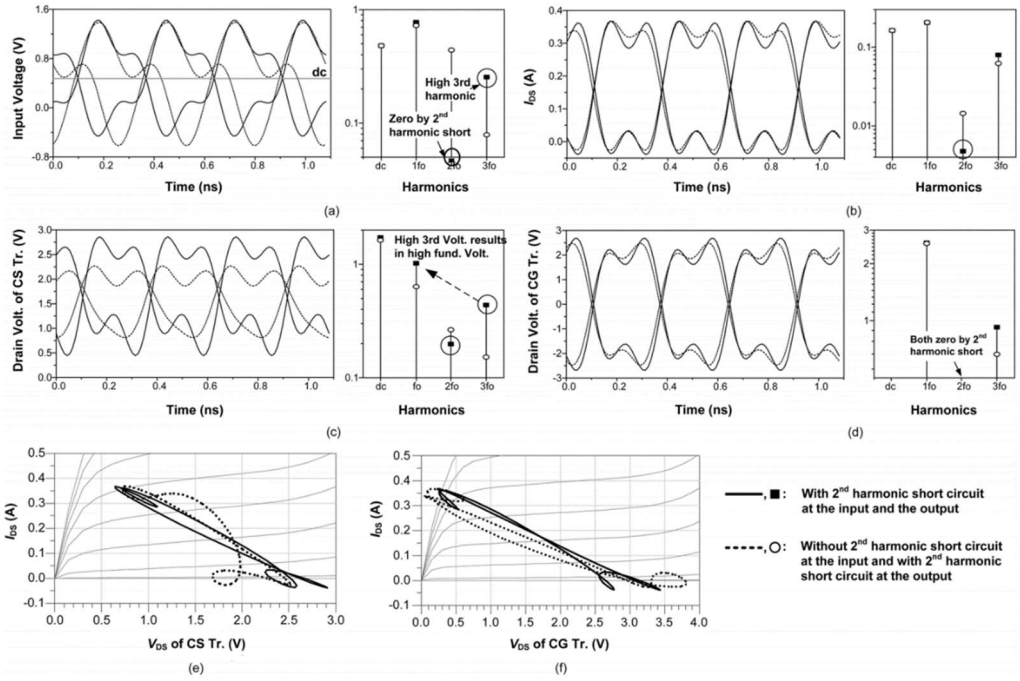


Figure 2-11. (a)-(d) Simulated voltage and current waveforms of the cascode transistor and their harmonics components of the waveforms. (e) Load line in the common source (CS) transistor. (f) Load line in the common gate (CG) transistor. The input harmonic short circuit reduces the distortion generated by the nonlinear input capacitances. It also increase output power at fundamental frequency in (c), thus P_{1dB} [5].

constant across the whole range of the input power level but increases with the increasing power level. Similarly, the capacitance between the gate and drain of the transistor also follows this behaviour in opposite phase, but with a bigger amplitude because the voltage at the drain is amplified. The distortion, which is created by those nonlinear capacitors, can be compensated by the second harmonic short circuit at the input, which is the gate of the

PA in Figure 2-10. As observed in Figure 2-12 [5], the input harmonic short circuit reduces the distortion generated by the nonlinear input capacitances.

On the other hand, the second harmonic short circuit at the output reduces the second harmonic voltage, hence improving the IMD3 and IMD5, shown in Figure 2-12.

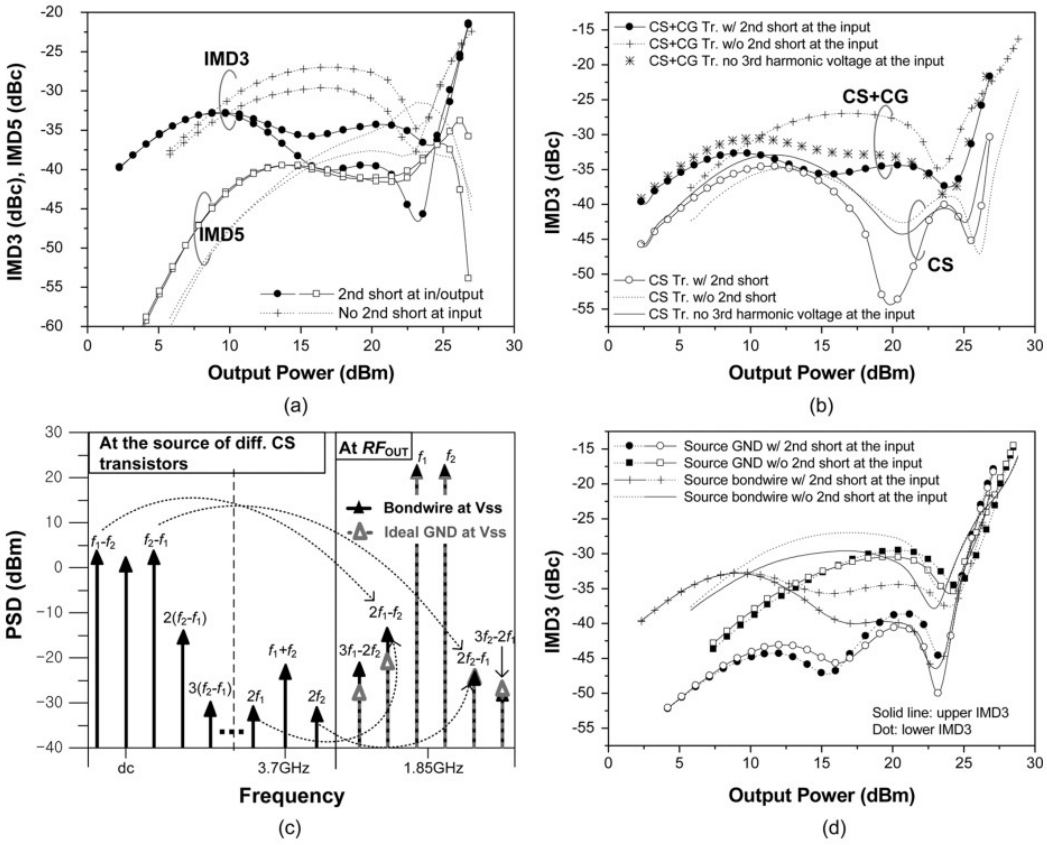


Figure 2-12. (a) Comparison of the simulated IMD characteristics of the PA with/without the second harmonic control circuits at the input. Both PAs have the second harmonic control circuits at the output. (b) Contributions of the CS and CG transistors to the distortion in the cascode structure. The impact of the third harmonic on IMD3 is also shown in the plot. (c) Simulated intermodulation power spectral density (PSD) at the output power of 23 dBm for the case with the second harmonic short at the input. (d) Reduced IMD3 imbalance by an ideal ground at the source terminal of differential CS transistors.

The efficiency of the devices also increases due to this improvement. A short circuit trap at the third harmonic component also improves IMD5 by eliminating the third harmonic. However, its contribution is much smaller than that of the second harmonic control circuit, as can be observed in Figure 2-12.

In another PA design in [53], a different harmonic termination technique at the common source node is adopted along with normal harmonic termination at the drain, as seen in Figure 2-13. The harmonic termination at the source effectively suppresses the second harmonic generated from the input and output.

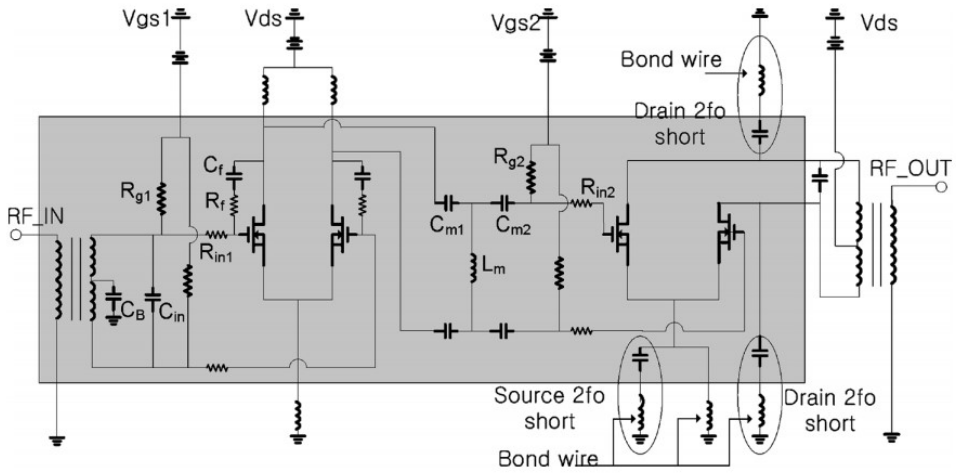


Figure 2-13. Schematic of harmonic tuned fully differential CMOS PA [53]. The harmonic termination technique at the common source node is adopted along with normal harmonic termination at the drain.

Linearity measurements from a two-tone test show that the power amplifier with the second harmonic termination improves the IMD3 and IMD5 over the amplifier without the harmonic termination by maximally 6 dB and 7 dB, respectively, as shown in Figure 2-14. From the OFDM signal test, the second harmonic termination improves the error vector magnitude (EVM) by over 40% for an output power level satisfying the 4.6% EVM specification.

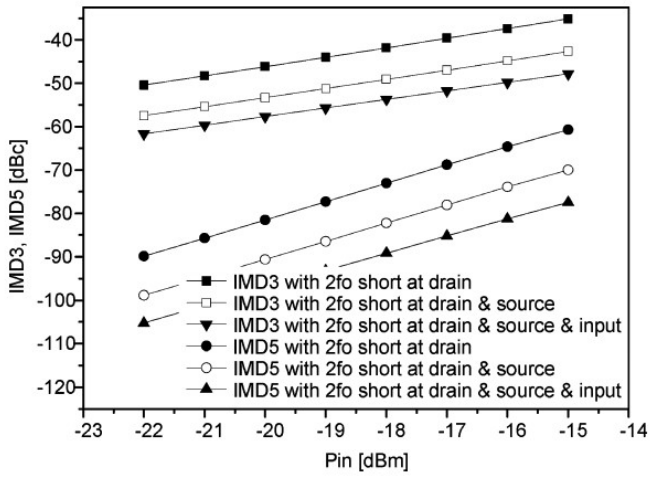


Figure 2-14. IMD3 and IMD5 comparisons for various methods of the second harmonic terminations. The power amplifier with the second harmonic termination improves the IMD3 and IMD5 by maximally 6 dB and 7 dB, respectively.

The second harmonic control techniques can be combined with the adaptive bias techniques to improve the linearity of the PA, as shown in [7].

Here, the second harmonic short circuits are deployed at the virtual ground of the common gate stage and common source stage, as shown Figure 2-15. The bond wires can

be utilized with metal-insulator-metal (MIM) caps to form a short circuit at the second harmonic frequency. As a result, the PA delivers a very high output power of 26.5 dBm and a PAE of 37.6% at 1.85 GHz.

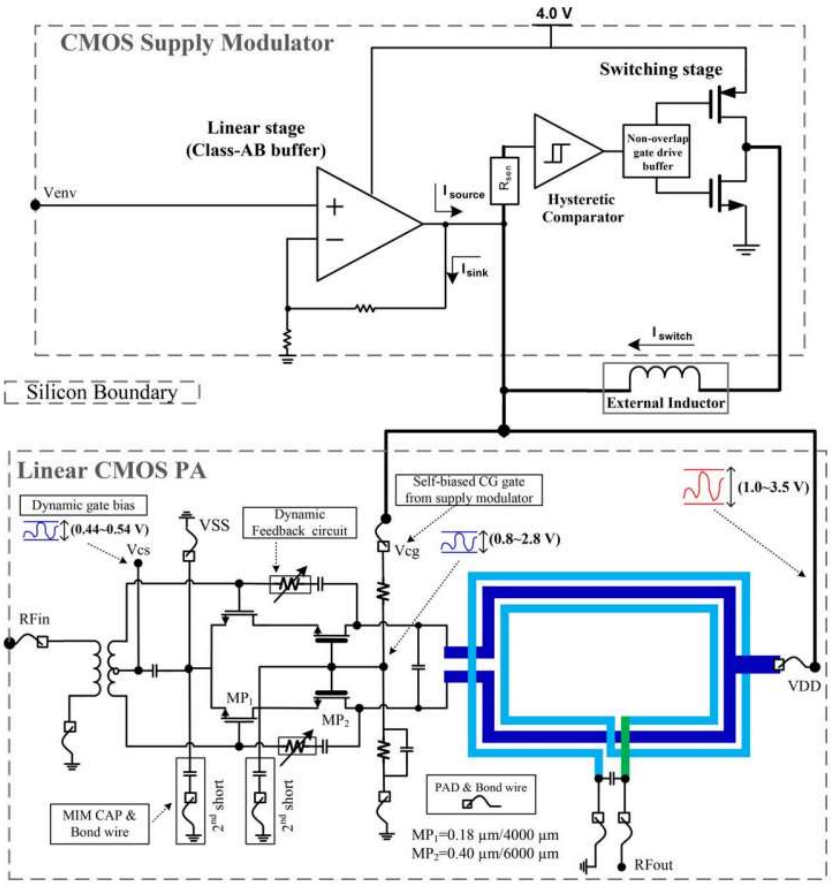


Figure 2-15. Second harmonic short circuit is in combination with the adaptive bias techniques [7].

In conclusion, the second harmonic suppression technique can improve intermodulation distortions, including IMD3 and IMD5. Furthermore, it can improve P_{1dB} and efficiency in some cases. The third harmonic suppression can also help improve intermodulation distortion, but the effect is much smaller than the second harmonic suppression. The technique is extensively deployed in literature because can be combined with other linear techniques such as adaptive bias circuit. The only drawback of this technique is that the MIM cap value is normally large in order to suppress the second harmonic. For example, the MIM cap value in the 5.8 GHz PA is about 10 pF. Hence, the size of the MIM cap is large as well. Therefore, the technique is only applied whenever there is enough space.

2.2.4 Summary

This section briefly describes the three most important parameters in designing the PA, namely P_{1dB}, power-added efficiency (PAE), and Rowlett stability factor K. The three parameters are used extensively in the PA design process in the Chapter 3. They are also used to judge performance of the PA. Then, the two linearity techniques including adaptive bias and second harmonic short circuit are reviewed carefully which focus on the existing issues.

The adaptive bias technique can extend P_{1dB} to some dB compared to the conventional counterparts of PAs. Furthermore, it can improve efficiency in some cases. The adaptive bias circuits normally are big and bulky, thus increasing design complexity and time. The adaptive bias circuits also consume considerable DC power. This can lead to the degradation of battery lifetime, which is not acceptable in modern RF transceiver designs with the demand of a longer operating time. This also does not comply with the current trending of miniaturization.

The second harmonic short circuit technique can improve intermodulation distortions, including IMD3 and IMD5. Furthermore, it can improve P_{1dB} and efficiency in some cases. The third harmonic suppression can also help improve intermodulation distortion, but the effect is much smaller than the second harmonic suppression. The technique is extensively deployed in the literature because can be combined with other linear techniques such as adaptive bias circuit techniques and multiple-gated transistor techniques. The only drawback of this technique is that the MIM cap value is normally large in order to suppress the second harmonic. For example, the MIM cap value in the 5.8 GHz PA is about 10 pF. Hence, the size of the MIM cap is large as well. Therefore, the technique is only applied whenever there is enough space.

2.3 Harmonic Suppression Antenna

Suppression of the higher order harmonics is of great interest in nowadays compact communication systems especially in systems with active integrated antennas (AIAs). In these systems, the antenna should suppress the higher-order harmonics to improve the PAE of the PA in the transmitter. On the receiver side, harmonic suppression is required to cancel out-of-band noise and interferences. A conventional approach to address these challenges is using filters in series with the antenna. However, this increases the total size, insertion loss, and implementation cost of the whole system and degrades the noise figure of the receiver. An alternative is to design an antenna with inherent out-of-band rejection capable

of rejecting unwanted radiations and suppressing higher-order harmonics. Table 2-2 shows the most prominent pros and cons of recent harmonic suppression techniques.

Table 2-2. Comparison of recent harmonic suppression techniques

Ref.	Rejection Techniques	Main Novelty	Pros	Cons
[54]	MIM cap and narrow microstrip line	A LC filter made by a MIM cap and a thin microstrip feed line is embedded completely inside the rectangular slot antenna	No change in size, radiation pattern and bandwidth Strong rejection capability	Thin lines may suffer from manufacturing errors
[55]	Narrow gaps and grounded double spur-line	Grounded double spur-line lines provide wide bandstop characteristics when inserted in a slot antenna	Strong suppression in harmonic bandwidth Wide bandwidth for slot antenna	Many narrow gaps and thin lines, making it prone to manufacturing errors Narrow operating bandwidth
[56]	Photonic bandgaps	Photonic bandgaps (PBGs) of various lattice shapes in the feed network provide well-behaved band-stop characteristics in a CPW loop slot antenna	Size is increased The operating bandwidth is enhanced.	Narrow rejection band Small PBGs prone to manufacturing errors
[57]	Defected ground slot (DGS)	The DGS, which works as a wideband band-stop filter, is coupled to the microstrip feed line in a slot antenna	Wide harmonic suppression bandwidth	Inadequate stopband rejection Size is increased
[58]	Coupling slot filters	Two coupling slots placed inside the radiating slot loop, forming two band-stop filters	Wide harmonic suppression bandwidth Size is decreased	Inadequate stopband rejection
[59]	Two folded L-shaped slots	Embedding two rectangular slots, which provides a band-stop at the third harmonic frequency, are etched into the open-ended tuning stub of the CPW transmission line and near the main radiation slots	Wide harmonic suppression bandwidth	Inadequate stopband rejection
[60]	Stepped-Impedance slot	Two stepped-impedance slot resonators, which shift the harmonic frequencies away, are connected to a short-circuited CPW feedline	Wide harmonic suppression bandwidth Strong size reduction	Inadequate stopband rejection Operating bandwidth is decreased
[61]	Wiggly-line band-stop filter	A wiggly-line band-stop filter structure applying the Bragg conditions is used	Strong rejection capability Size reduction	Very narrow operating bandwidth Many narrow gaps, making it prone to manufacturing errors

A metal-insulator-metal (MIM) capacitor, formed by a T-shaped feeding and a grounded stub and a thin microstrip inside a slot antenna, is used to suppress the higher-order out-of-band harmonics [54]. The harmonic supersession was achieved without changing the size, bandwidth, and radiation pattern when compared to the conventional counterpart antenna. Another technique in [55] used grounded conductor lines embedded in the dual slot antenna, resulting in a strong suppression in the harmonic bandwidth

including second and third harmonic frequencies. This antenna also creates two resonance frequencies, providing a wide bandwidth. Nevertheless, the design is complicated with many narrow gaps and thin lines, making it prone to manufacturing errors. Furthermore, the fractional bandwidth (FBW) of the antenna is only 18.5%, which is not suitable for wideband applications. A broadband coplanar waveguide (CPW)-fed loop slot antenna combined with photonic bandgaps (PBGs), which provides a stop-band of various lattice shapes in the feed network was proposed in [56] for harmonic suppression. The harmonic suppression capability and bandwidth are enhanced with the PBG structures. However, the PBGs are placed completely outside the antenna, failing to achieve the size reduction goal. In addition, the harmonic suppression bandwidth is narrow which covers only the second harmonic frequency. In [57], a wideband harmonic suppression is achieved using the defected ground slots (DGSs), which provides a wide stop-band, coupled to the microstrip feed line in a narrowband antenna. A major part of the DGS is placed outside the main radiating slot, leading to an increase in the overall size of the antenna. Moreover, the return loss in the rejection region reaches 2.5 dB, showing inadequate stopband rejection. Other techniques such as the slot coupled filter [58], folded L-shaped slots [59], and stepped impedance slots [60] were used to suppress harmonics without increasing the overall size of the main antenna. However, all these techniques show low return losses, and thus, inadequate suppression of higher order resonances in the rejection region. Only the wiggly-line band-stop filter technique [61] achieves good performance in the rejection region, but at the expense of a narrow operating bandwidth. Furthermore, the antenna comprises several narrow gaps, making it prone to manufacturing errors.

In this section, only the harmonic suppression techniques, namely defected ground structure, stepped slot, thin microstrip line, and metal-insulator-metal (MIM) cap are reviewed in detail. All these techniques have the capability of suppressing harmonic frequencies with the potential of maintaining or reducing the size of the main radiating element. These techniques can be combined, leading to new harmonic suppression techniques with superior performance. These new techniques are applied in all three of the harmonic suppression antenna designs.

2.3.1 Basic Parameters

This section describes the two most important parameters of the harmonic suppression antenna, namely gain and return loss. These parameters are used to judge the harmonic suppression capability of a harmonic supersession antenna.

Electromagnetic radiation of an antenna is created by alternating currents, which is composed of accelerating electrons. The magnitude of electromagnetic radiation is described using the decibel unit. The expression dBi is used to define the gain of an antenna system relative to an isotropic radiator at radio frequencies. Suppose an isotropic antenna creates an electromagnetic field of intensity I_Q at the same distance, then the gain G of antenna A, in dBi, is:

$$G = 10log_{10}\frac{I_A}{I_Q} \tag{2.3}$$

where I_A is the electromagnetic field of intensity of antenna A.

For example, an isotropic antenna has a gain of 0 dBi.

A high gain antenna will focus most of its power in a direction, while a low-gain antenna will radiate over a wide angle. A high gain antenna will cover a longer range and better signal quality, but its direction must be taken into a careful consideration. A low-gain antenna will cover a shorter range, but the orientation of the antenna is not important.

The term radiation pattern refers to a variation of the radiated power of the antenna as a function of the direction away from the antenna. This power variation as a function of the arrival angle is observed in the antenna's far field, for $r \gg 2D^2/\lambda$, with D being the largest dimension of the antenna and λ is the wavelength. The gain of an antenna is just the amount of power in the direction of maximum radiation divided by the average power.

Antenna impedance is an important parameter, which generally is a complex number. At resonating frequencies, the imaginary is zero or close to zero. The real part is optimized to the same value with the impedance of the transmitter or receiver, normally is 50 Ohm. The process to optimize the desired impedance is called impedance matching. Return loss can be used to judge if the impedance matching meets the specification or not. It is described as the dB ratio between incident power P_i and reflected power P_r in the port of the antenna, as follows:

$$R_L(dB) = S_{11}(dB) = 10log_{10}\frac{P_i}{P_r} \tag{2.4}$$

For instance, if the return loss of the antenna is close to 0 dB, this means that the antenna is completely unmatched, and the antenna is not radiating at that frequency. If the return loss is 10 dB, this means that 90% of the power is radiated or absorbed and converted into

heat inside the antenna. The 10-dB return loss is practically acceptable as a "rule of thumb" for antenna design.

The return loss of a harmonic suppression antenna is expected above 10 dB in the fundamental frequency, whereas it should be as close as possible to 0 dB at higher order harmonic frequencies. The gain should follow the same manner with the return loss, i.e. it is expected to have a high value, ≥ 0 dBi at operating frequency whereas it should be much smaller at higher order harmonic frequencies.

2.3.2 Defected Ground Structure

The works in [62] [57, 63] shows that the defected ground structure (DGS) can reduce higher order harmonics in patch antennas and slot antennas. The DGS works as a stopband filter when coupled with the microstrip feed line of the antenna. It increases the impedance of the microstrip feed line at higher harmonic frequencies while maintaining the impedance at fundamental frequencies.

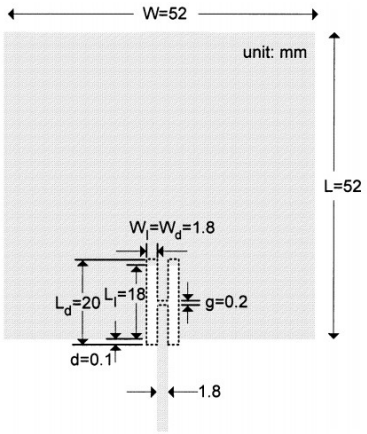


Figure 2-16. Top view of the proposed DGS patch antenna. A H-shaped DGS is etched at the inset cut of the patch antenna.

A H-shaped DGS is used with the square patch antenna at 1.82 GHz [62] to provide harmonic suppression for the second and the third harmonic components. Here, the DGS is etched on ground plane at the position of the inset cut of the patch antenna. Figure 2-16 shows the configuration of the DGS microstrip harmonic supersession antenna.

The DGS works as a bandstop filter right at the feed of the antenna and it does not alter the gain of the antenna. The gain of the harmonic suppression antenna is 4.8 dBi, which is almost equal to the gain of 4.9 dBi of the conventional patch antenna without DGS.

The return losses of the patch antenna with and without DGS in the simulation and measurement is shown in Figure 2-17. It is observed that the DGS suppresses all the

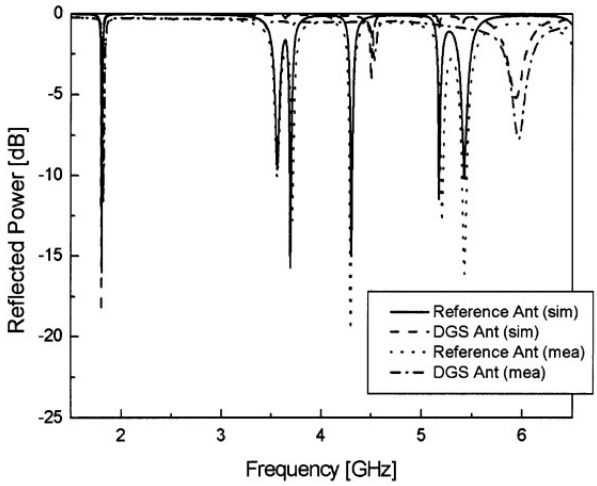


Figure 2-17. Simulated and measured return losses. The DGS antenna provides low return loss at higher order harmonic frequencies at the expense of a small reduction in operating bandwidth.

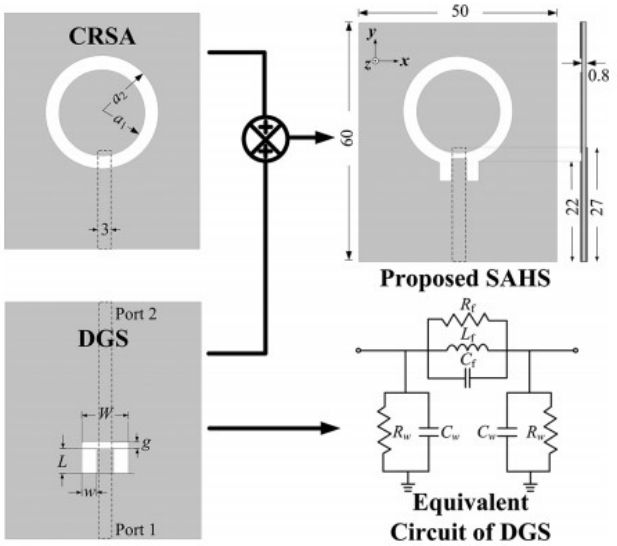


Figure 2-18. Design evolution of proposed slot antenna with harmonic suppression [57]. An inverted U-shaped DGS is inserted into a circular ring slot antenna.

resonance frequencies from 2 GHz to 5.5 GHz. From the radiation pattern measurement results, the DGS provides 20 dB suppression at the second harmonic frequency compared to the patch antenna without DGS while the power level at the third harmonic frequency is too small to detect.

In another work, the DGS technique is applied to a circular ring slot antenna (CRSA) [57]. By integrating an inverted U-shaped DGS into the circular ring slot, shown in Figure 2-18, harmonic suppression over a wide bandwidth between 3 and 9 GHz can be achieved. In this design, the DGS is combined very closely with the slot antenna and thus, no apparent

cascaded band stop filter is observed, as shown in Figure 2-18. Furthermore, the proposed antenna is simple in structure and easy to fabricate.

The working principles of the DGS are explained in Figure 2-19. By observing the insertion loss S_{21} of the standalone DGS structure, a stop band approximately between 3 and 8.6 GHz was observed. Therefore, loading the DGS into the CRSA will not have much effect on fundamental frequency, whereas it suppresses higher resonance frequencies below -3 dB (half power) threshold.

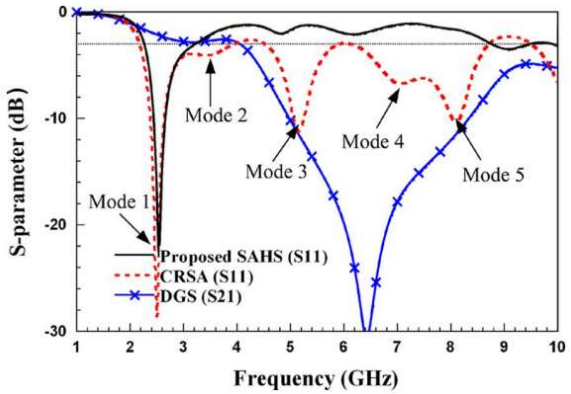


Figure 2-19. Simulated S_{11} of proposed antenna and CRSA, and S_{21} of DGS [57]. The inverted U-shaped DvGS provide a stopband between 3 and 8.6 GHz in expense of small reduction in operating bandwidth.

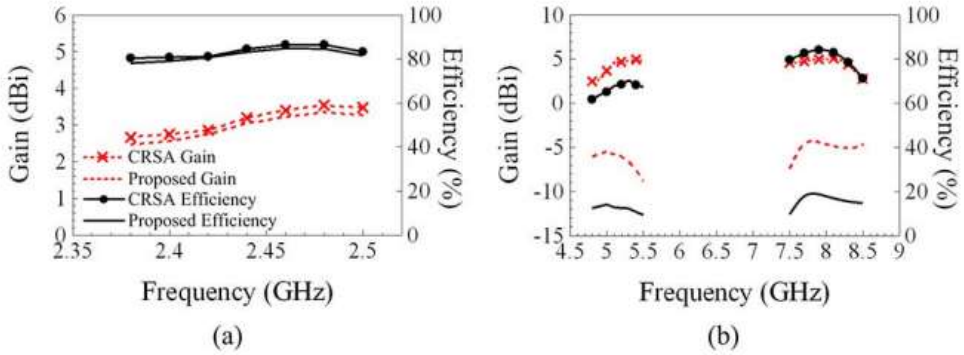


Figure 2-20. Measured peak gain and efficiency variation of the proposed antenna and CRSA [57] across (a) the fundamental frequency and (b) the second and the third harmonic frequencies.

Furthermore, the reduction in gain between 4.8 and 5.5 GHz (the second harmonic) and 7.5 GHz and 8.5 GHz (the third harmonic) is 9 dB and 12 dB as shown in Figure 2-20, respectively.

The work in [62] shows a good rejection, ~1dB, in harmonic region, but with a very limited operating bandwidth. The work in [57] achieves a better operating bandwidth of 8.42 %. Both works achieve harmonic supersession at the expense of a smaller operating bandwidth, compared to the conventional counterpart antennas. Furthermore, a major part of the DGS is placed outside the main radiating slot, leading to an increase in the overall

size of the antennas. The return loss in the rejection region reaches only 2.5 dB, showing inadequate stopband rejection.

In conclusion, the DGS works as a bandstop filter, which can be integrated with patch or slot antennas to provide suppressions across a wide frequency rage. However, in all of the reviewed works in the literature, the DGSs were placed partially or totally outside the antenna. As a result, the size of the modified antennas increases. Furthermore, the DGS alone does not provide enough suppression as the return loss in the rejection range still has some bumps or resonances. The bandwidths of all the modified antennas are reduced compared with its conventional counterpart antennas.

2.3.3 Stepped Slot

The work in [60] is the only work in the literature which shows that the stepped slot technique can achieve a harmonic suppression in coplanar waveguide (CPW) slot antennas. Furthermore, the technique also reduces the size of the slot antenna by 32%. Different from the DGS technique, in which the DGS acts as a bandstop filter, the stepped slot technique alters the impedance at the exact the second time and the three times of the fundamental frequency due to its stepped structure. The imaginary parts of the antenna's impedance are not close or equal to zero at those frequencies but at higher frequencies. Therefore, the return losses at the exact harmonic frequencies are small. Hence, the stepped CPW slot antenna in [60] is a harmonic suppression antenna. The geometry of the stepped impedance slot antenna can be seen in Figure 2-21. Here, the antenna is composed of two stepped slot resonators which are fed by a CPW.

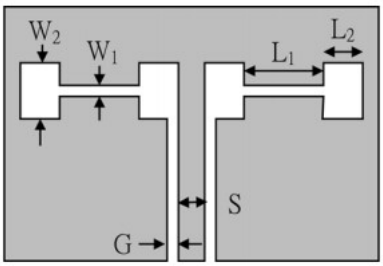


Figure 2-21. Configuration of the CPW-fed inductively coupled slot antenna proposed in [60].

At the fundamental frequency of 4.5 GHz, the stepped resonator achieves the same zero input impedance of the uniform slot antenna. For higher frequencies, the uniform and stepped-impedance resonators behave differently. The return loss of the proposed antenna across frequency is depicted in Figure 2-22.

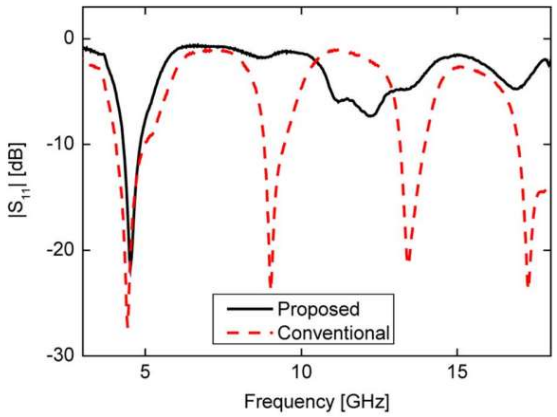


Figure 2-22. Measured $|S_{11}|$ of the proposed and conventional uniform antenna [60]. The proposed antenna shows low return loss at high-order harmonic frequencies. The data also shows that the operating bandwidth of the harmonic suppression antenna reduces compared to the conventional uniform antenna.

It is obvious that the proposed antenna provides a small return loss at the second, the third, and the fourth harmonic frequencies. However, the return loss in the rejection region reaches 7 dB, showing very weak stopband rejection. The operating bandwidth of the harmonic suppression antenna also reduces compared to the conventional uniform antenna.

In conclusion, the stepped slot suppresses the higher harmonic components by altering impedance at these frequencies, reducing their return losses. Furthermore, it can help to reduce the size of the antenna. However, the antenna must be a slot antenna with a specific stepped shape. It also does not provide strong suppression across the whole range of rejection frequency. The return loss at higher frequency than operating frequency still has some bumps or resonances. As a result, it cannot filter out all the unwanted out-of-band frequencies.

2.3.4 Thin Microstrip Line and MIM Cap

The works in [54] [64] [65] show that a thin microstrip line and a metal-insulator-metal (MIM) capacitor can achieve harmonic suppression in both patch and slot antennas. In three cases, the thin microstrip lines act like a lumped inductor and the MIM caps play a role like a lumped capacitor at high frequency, which is similar to an inductor and capacitor in a LC lowpass filter.

The two antennas [64] show that the thin microstrip line and a metal-insulator-metal (MIM) capacitor are effectively utilized to suppress higher order harmonic components in patch antenna, as shown in Figure 2-23. The antenna in Figure 2-23(a) [64] utilizes a compact microstrip resonant cell (CMRC). The CMRC composes of some thin microstrip lines which add to the serial inductance and gaps which add to the shunt capacitance of the

microstrip line. Thus, CMRC can provide harmonic suppression until the second harmonic frequency, as can be seen in Figure 2-23(b) and (c).

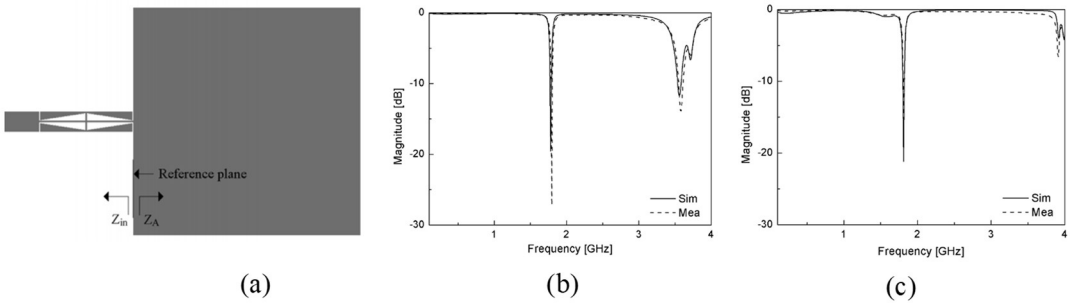


Figure 2-23. (a) Schematic diagram of a patch antenna [64] with a compact microstrip resonant cell (CMRC).(b) S-parameters of the conventional antenna. (c) S-parameters of the harmonic suppression antenna. Comparison between that (b) and (c) show that the CMRC can provide stopband until the second harmonic frequency.

In the harmonic supersession antenna shown in Figure 2-24, a harmonic suppression structure, which comprises a single open-ended stub with a pair of dumbbell-DGSs, is used to achieve a wide stopband. The DGS acts like a serial inductor and the open-ended stub plays a role like a shunt capacitor. Thus, the harmonic structure can be equivalent to an LC filter. As a result, the antenna can provide a stopband over the second and third harmonic frequencies.

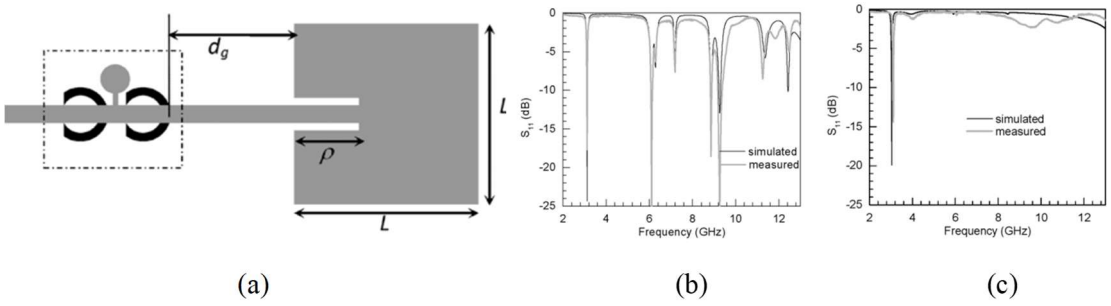


Figure 2-24. (a) (b) Schematic diagram of inset fed square patch antenna [65] fed by a DGS integrated microstrip line and an open stub (MIM cap). (b) S-parameters of the conventional antenna. (c) S-parameters of the harmonic suppression antenna. Comparison between that (b) and (c) show that the DGSs and MIM cap can provide stopband until the third harmonic frequency

However, in the two antennas, both the thin microstrip line and the MIM cap are placed completely outside the antenna, failing to achieve the miniaturization goal.

The thin microstrip line and MIM cap can also be used in a slot antenna to provide an effective stopband over the second and the third harmonic frequencies. An example of a wideband slot harmonic suppression antenna [54] is shown in Figure 2-25.

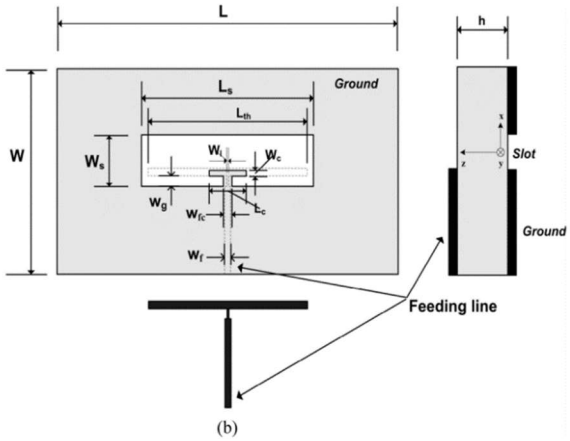


Figure 2-25. The T-shaped fed slot harmonic suppression antenna [54]. A compact harmonic suppression structure is inserted totally inside the main radiating slot.

A magnified view of the harmonic suppression structure in the input feedline region is shown in Figure 2-26. The thin microstrip line acts like an inductor. Together with the MIM cap formed by the below ground stub and the upper microstrip line, the harmonic structure acts like a LC low pass filter, filtering out the higher harmonic frequencies.

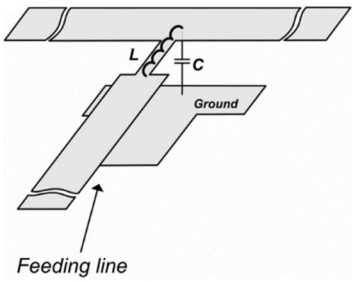


Figure 2-26. Zoomed view of harmonic suppression structure of input feedline region [54]. The thin microstrip line and the MIM cap acts like a LC low pass filter.

The return loss of the proposed antenna is shown in Figure 2-27. The bandwidth does not change when the harmonic suppression structure is attached into the slot. The size and the gain at fundamental frequency of the harmonic suppression antenna is the same as that of the conventional slot antenna.

The thin microstrip line and MIM capacitor are also used in another work of the harmonic suppression patch antenna [64].

In conclusion, the thin microstrip line and MIM capacitor can be embedded into a wide slot antenna to suppress the frequency higher than the operating frequency. It does not increase the size of the antenna while maintaining bandwidth and gain. The thin microstrip line and MIM capacitor can also be utilized in patch antennas to provide harmonic suppression. However, in both the two patch antennas, the thin microstrip line and MIM

cap are placed totally outside the antenna, failing to achieve miniaturization goal. Furthermore, the thin microstrip line may increase manufacturing error.

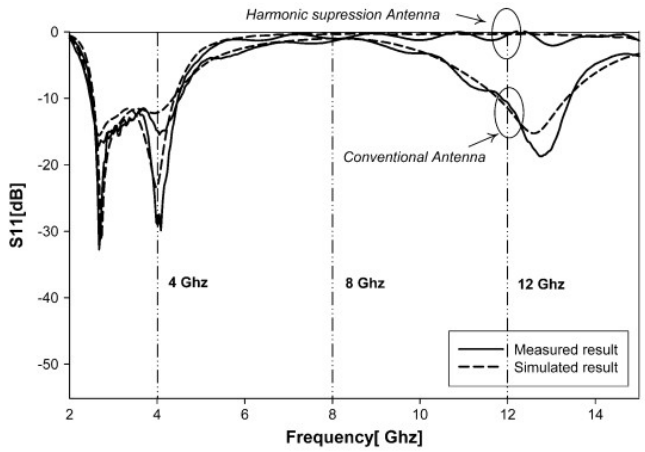


Figure 2-27. The simulated and measured return losses of the T-shaped slot antenna [54]. The proposed harmonic supersession antenna has small return loss at the second and third harmonic frequencies.

The thin microstrip line and MIM capacitor are also used in another work of the harmonic suppression patch antenna [64].

In conclusion, the thin microstrip line and MIM capacitor can be embedded into a wide slot antenna to suppress the frequency higher than the operating frequency. It does not increase the size of the antenna while maintaining bandwidth and gain. The thin microstrip line and MIM capacitor can also be utilized in patch antennas to provide harmonic suppression. However, in both the two patch antennas, the thin microstrip line and MIM cap are placed totally outside the antenna, failing to achieve miniaturization goal. Furthermore, the thin microstrip line may increase manufacturing error.

2.3.5 Summary

This section briefly describes the two most important parameters of harmonic suppression antennas, namely gain and return loss. These parameters are used to judge the harmonic suppression capability of a harmonic supersession antenna. Then, the three harmonic suppression techniques namely DGS, stepped slot, and thin microstrip line and MIM cap are reviewed carefully which focus on the existing issues of those techniques.

The DGS works as a bandstop filter, which can be integrated with patch or slot antennas to provide suppressions across a wide frequency rage. However, in all of the reviewed works in this section, the DGSs were placed partially or totally outside the antenna. As a

result, the size of the modified antennas increases. Furthermore, the DGS alone does not provide enough suppression as the return loss in rejection range still has some bumps or resonances. The bandwidths of all the modified antennas are reduced compared with its conventional counterpart antennas.

The stepped slot suppresses higher harmonic components by altering impedance at these frequencies, reducing their return losses. Furthermore, it can help reduce the size of the antenna. However, because the technique uses a stepped shape, the modified antenna must be a slot antenna with a specific stepped shape. It also does not provide strong suppression across the whole range of rejection frequency. The return loss at a higher frequency than the operating frequency still has some bumps or resonances. As a result, it cannot filter out all the unwanted out-of-band frequencies.

Finally, the thin microstrip line and MIM capacitor can be embedded into a wide slot antenna to suppress frequencies higher than the operating frequency. It does not increase the size of the antenna while maintaining bandwidth and gain. The thin microstrip line and MIM capacitor can also be utilized in patch antennas to provide harmonic suppression. However, in both the two patch antennas, the thin microstrip line and MIM cap are placed completely outside the antenna, failing to achieve the miniaturization goal. Furthermore, the thin microstrip line may increase the manufacturing error.

2.4 Full-Duplex Antenna

The in-band full-duplex (IBFD) operation is of great interest in compact communication systems due to its capability to double spectra efficiency [27]. An IBFD system enables transmitting and receiving on the same frequency simultaneously. However, IBFD systems are still not widely used due to self-interference, in which radio signals from its own transmitter (TX) can be received by the receiver (RX). Here, the power of the self-interference (SI) signal can be a million times higher than the power of the received signal. Therefore, many techniques have been proposed to improve the isolation between collocated TX and RX. Due to passiveness, hence, simplicity, antenna isolation techniques are in high demand. They can also help reduce the complexity of self-interference cancelation in the digital domain.

There are several antenna isolation techniques such as orthogonal polarization [66, 67], even-mode and odd-mode excitation in CPW [41, 68], differential feeding [29, 69, 70], coupler [42-44], parasitic /decoupling resonating structures [45, 71], and reflective termination.

The orthogonal polarization method using two separated radiating elements in [66, 67] can achieve ~ 25 dB isolation, which is considered low in full-duplex applications. In addition, the two radiating elements occupy a large space, which is not suitable considering the demand for miniaturization. However, the method can achieve a more than 30%

Table 2-3. Comparing recent high isolation techniques

Ref.	Isolation techniques	Main Novelty	Pros	Cons
[66, 67]	Orthogonal polarization	Weak coupling between orthogonal electrical fields	Wide operating bandwidth (>30%)	Low isolation ~ 25 dB Large size
[41, 68]	CPW	Isolation between even mode and odd mode in CPW structure	Small size Wide operating bandwidth (>30%)	Low isolation ~ 20 to 30 dB
[69]	Differential feeding	Geometrical symmetry of the two spiral antennas to cancel the coupled TX voltages at the RX port	High isolation ~40 to 50 dB Wide operating bandwidth	Complex and costly 3D design
[42, 43] [44]	Coupler	Utilizing isolation of common and differential mode in a coupler	High isolation ~35 to 50 dB	Narrow bandwidth Big size
[45]	Decoupling	Insert decoupling structures between two antennas	High isolation ~ 50 dB	Big increasement in size
[46]	Reflective Term.	Applying a reflective termination in the third port to cancel out the coupling between the other two ports	High isolation 35.9 -46.5 dB	Narrow bandwidth Not small size

operating bandwidth. Another method [41, 68] using a single radiating element, thus a smaller space, utilizes the even mode and odd mode in CPW to achieve ~ 20 to 30 dB isolation between the two ports. This method also can achieve a more than 30% operating bandwidth.

The differential feeding method in [69] uses geometrical symmetry of the two spiral antennas to cancel the coupled TX voltages at the RX port, achieving an isolation of about 40 to 50 dB across a wide bandwidth. However, it requires a complex and costly 3D design. The method in [29, 70] also uses a differential feeding method but for rectangular patch antennas. The isolation is improved further, up to 90 dB by using additional 3dB/180^{o} ring hybrid couplers. However, this isolation value can only be achieved in a very limited bandwidth. Moreover, the feeding network, which includes couplers, occupies a critically large area. Couplers are also used in [42-44] to improve isolation up to ~35 dB to 50 dB. These couplers form a differential structure using a half wavelength delay line between their two ports, leading to opposite phases. Nevertheless, the total size of PCB or the

number of fabricated layers must be increased to embed the couplers. The decoupling structures in [45, 71], which basically are resonators, increase the isolation up to 50 dB. This method uses two separated radiating elements plus resonators, thus significantly increasing the size. The antenna in [46] uses reflective termination method. The isolation is about 35.9 -46.5 dB. However, the isolation is not constant across operating bandwidth. Furthermore, the antenna system has two separated antennas with two layers, leading to increasement in size and cost. Finally, the operating bandwidth is ~9% only.

In this section, three isolation techniques, namely coupler, coplanar waveguide configuration, and reflective termination are reviewed in detail. The coupler and coplanar waveguide configuration techniques are extensively studied in the literature due to their wide operating bandwidth. The reflective termination has recently emerged as a potential candidate due to its small increasement in size while achieving a moderate operating bandwidth and isolation.

2.4.1 Basic Parameters

The most important parameter of a full-duplex antenna system is the isolation between

Figure 2-28. Two-port antenna network.

two ports of the antenna system, which is shown in Figure 2-28. Isolation can be expressed as S_{12} or S_{21}, which is the power from antenna 1 delivered to antenna 2 and vice versa, respectively.

If S_{21} =0 dB, it is implied that all the power delivered to antenna 1 ends up at the terminals of antenna 2. If S_{21} =10 dB, then if 1 Watt (or 0 dB) is delivered to antenna 1, then -10 dB (0.1 Watts) of power is received at antenna 2. Similarly, if S_{21} =50 dB, then -50 dB (0.000001 W or 0.001 mW) of power is received at antenna 2. To satisfy the requirement of a full-duplex antenna, S_{21} or S_{12} should be as large as possible. The isolation goal of the proposed design is larger than 30 dB.

2.4.2 Coupler

The works in [42-44] show that couplers can improve isolation between two ports of antenna systems by up to 35 dB. These antenna systems utilize a DGS and the high isolation and perfect balance of microstrip rat-race couplers or 180º hybrid couplers to improve the isolation between two separated antennas.

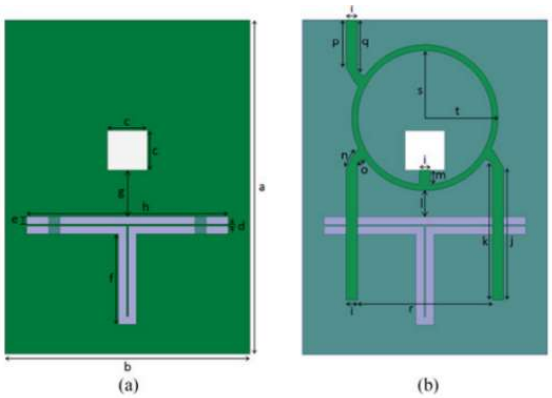


Figure 2-29. (a) Bottom and (b) top layers of the proposed antenna with a T-shaped DGS and a coupler [42].

The monopole array antenna in Figure 2-29, which comprises a rat-race coupler, a T-shaped DGS, and two monopole antennas is proposed in [42] to achieve a measured isolation (S_{21}) of 35 dB in a reflective environment.

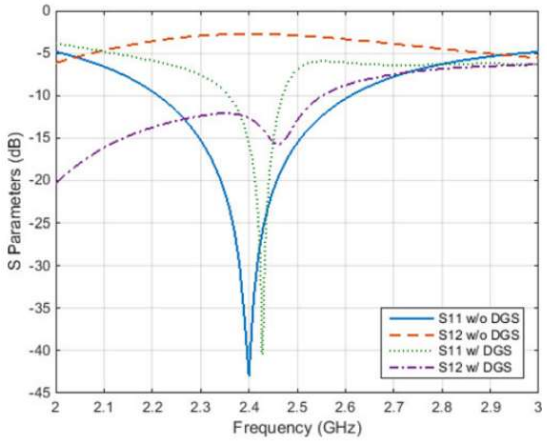


Figure 2-30. Effect of DGS on S-parameters [42]. The DGS improves the isolation S_{21} by 12 dB.

When the first monopole antenna is excited, there is an induced current on the second monopole antenna. Therefore, a T-shaped DGS which is etched in the ground plane is used to reduce S_{21} by collecting surface currents along its shaped turns, thus keeping the induced current off the second monopole. The effect of DGS on S-parameters of the array antenna is described in Figure 2-30. The DGS improves isolation S_{21} by about 12 dB, meaning self-interference is reduced.

Then, a ring hybrid is incorporated symmetrically into the design to further improve isolation up to 35 dB, as described in Figure 2-31. The two symmetric and identical monopole antennas are connected to ports 2 and 4 of the hybrid, making the reflected powers equal and out-of-phase. These powers combine destructively at the receiving port, leading to a drastic increment in isolation. Here, the coupler is connected in parallel with

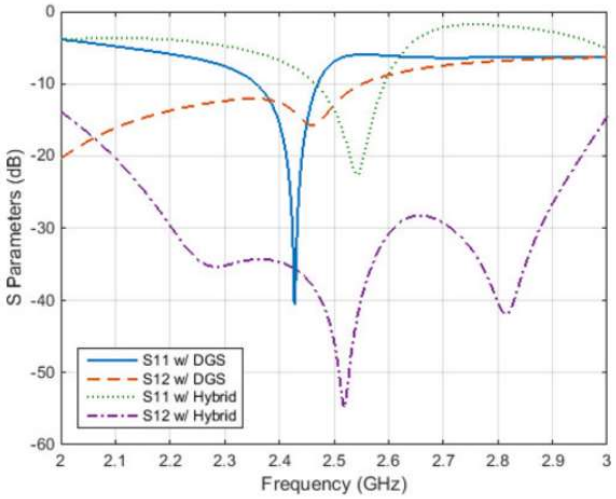


Figure 2-31. Effect of hybrid on S-parameters [42]. The data show that the hybrid improves isolation to 35 dB.

the antenna since the receiving and transmitting signals are extracted from the sum port and differential port of the hybrid. The isolation will be lower or equal to the isolation of the hybrid because of a parallel configuration. As a result, a measured isolation greater than 35 dB in 5.4 % bandwidth is achieved in a reflective room.

In another work [43], a probe-fed patch antenna with 180^{o} ring hybrid is proposed for in-band full-duplex applications. A patch antenna is printed on one substrate, and a ring hybrid is printed on a second substrate. The ring hybrid is designed in the splitter/combiner configuration. In this design, the receiver port is directly connected to the patch antenna through a microstrip line while the difference input port of the hybrid was used as the transmit port. The patch antenna was differentially excited using the two output ports of the hybrid, as shown in Figure 2-32 . Here, the coupler is connected in series with the patch antenna since the receiving signal is extracted from the patch antenna while the transmitting signal is supplied into the differential port of the hybrid. In a serial configuration, the isolation of the whole system is almost equal to the sum of the isolation of the two members, i.e. patch antenna and coupler.

Simulated and measured S-parameters in Figure 2-33 show an isolation level of 50 dB or higher across 2.3 % bandwidth around 2.4 GHz. The isolation in this work is higher than the isolation in [42] because of the serial configuration between the coupler and the antenna.

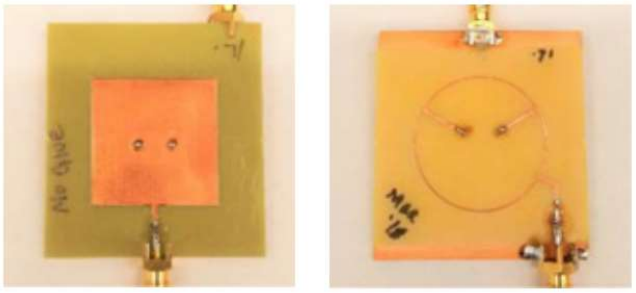


Figure 2-32. Fabricated prototype for proposed antenna [43]. The hybrid is connected in series with the antenna to improve the isolation.

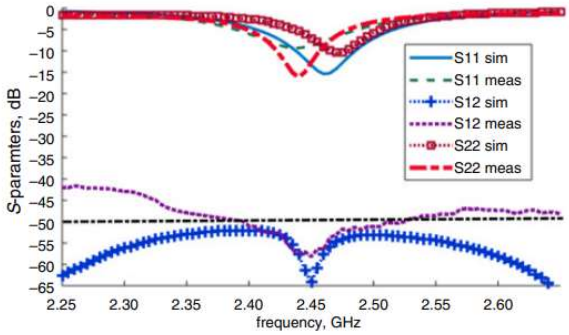


Figure 2-33. Simulated and measured S-parameters [43]. The data shows a 50 dB isolation with limited bandwidth.

In conclusion, couplers can be integrated with antennas to improve isolation. The serial configuration can achieve a 50-dB isolation, which is better than a 35-dB isolation in a parallel configuration. However, the integration of the coupler into the antenna normally increases the size of the antenna or increases the number of substrate layers, which does not follow the current trend of miniaturization or low-cost substrate. Moreover, the high isolation only maintains the narrow bandwidths of 5.4 % in [42] and 2.3% in [43].

2.4.3 Coplanar Waveguide Configuration (CPW)

The works in [41] [68] show that an even mode and odd mode of a CPW structure can be exploited to have an isolation level of about 20 dB to 30 dB between two ports of the antenna systems. Furthermore, the CPW antenna can achieve a wide bandwidth, more than 20% at both ports, calculated with centre frequency.

A compact and planar dual-antenna structure [68] is reported which combines a printed monopole and a half-slot antenna to provide dual polarization.

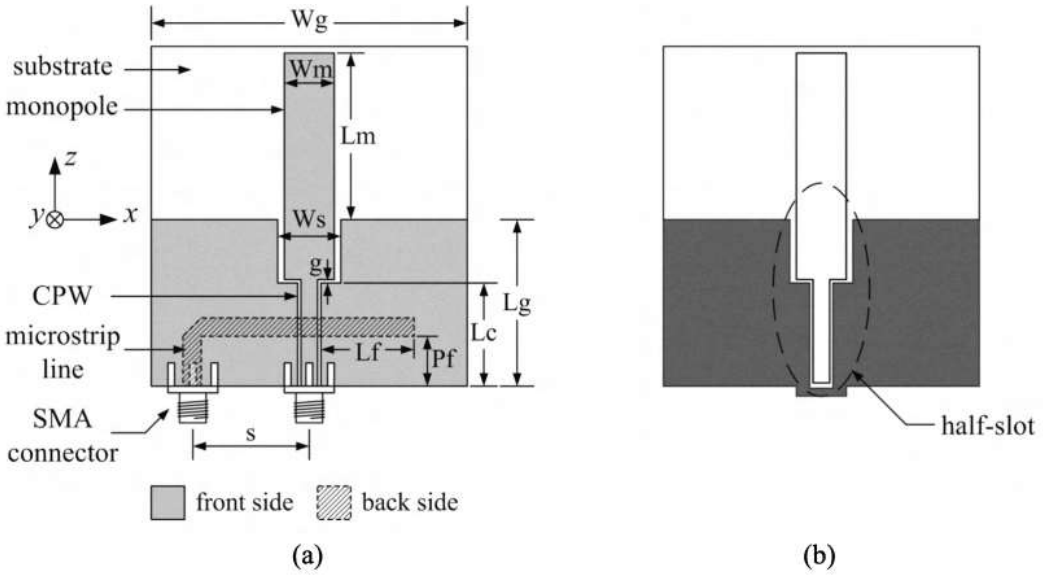


Figure 2-34. (a) Configuration of the antenna which includes two SMA ports [68]. (b) Schematic sketch of the half-slot.

The antenna combines a printed monopole fed by a coplanar waveguide (CPW) and a half-slot fed by a microstrip line to provide vertical and horizontal polarization respectively. Low mutual coupling is guaranteed due to the different current modes excited by the two ports.

By welding a SMA connecter to the CPW, the two halves of the ground will be shorted at the bottom and form a half-slot which is also about one quarter wavelength long, as illustrated in Figure 2-34(b).

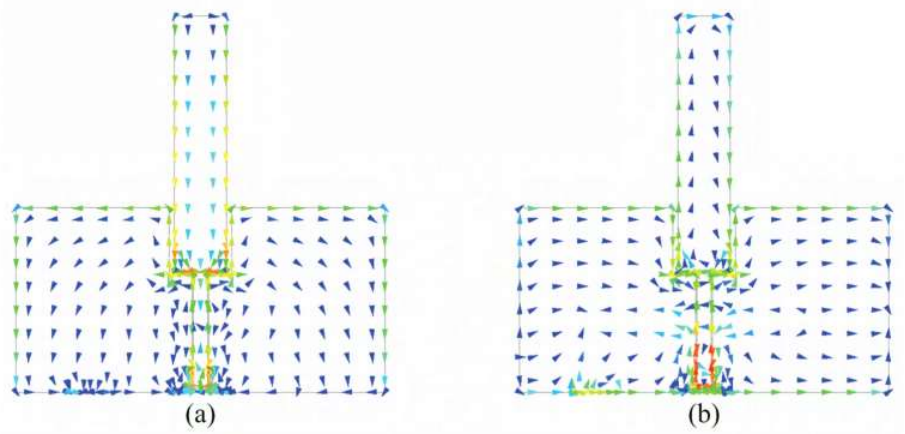


Figure 2-35. Simulated current distribution [68]: (a) the monopole is excited; (b) the half-slot antenna is excited.

Figure 2-35 shows the simulated current distribution at 2.35 GHz with one port excited and the other terminated. When the monopole is excited, the current flows on the left and right halves are mostly symmetrical and in phase, whereas when the half-slot antenna is excited, the current flows on the two halves are mostly 180 degrees out of phase. Therefore,

the two ports of the proposed antenna can be isolated although the monopole and the half-slot antenna are closely packed together.

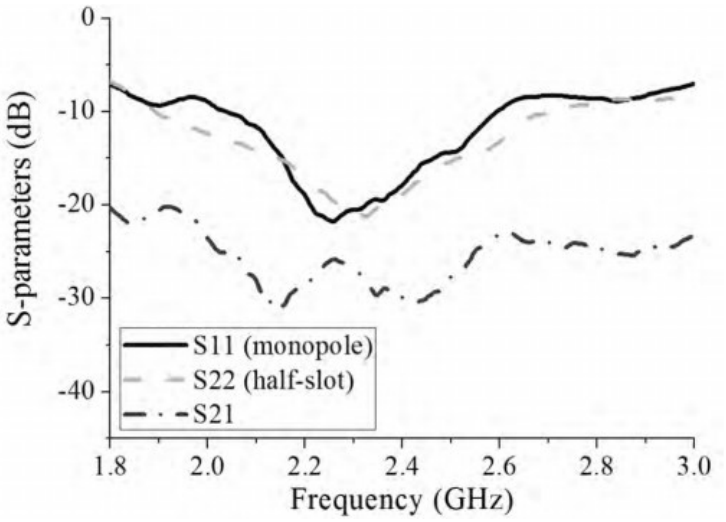


Figure 2-36. Measured S-parameters show an isolation of better than 23 dB across the measured bandwidth [68].

Figure 2-36 shows the measured S-parameters. The measured 10 dB return loss bandwidths are 2.045-2.59 GHz (23.5%) for the monopole and 1.895-2.7 GHz (35%) for the half-slot antenna. The mutual coupling between the two ports is less than -23 dB across the common bandwidth.

A CPW-fed slot antenna [41], which is a wide square slot antenna, comprises two ports, one a microstrip port and the other a CPW port. The geometry of the antenna is shown in Figure 2-37. The square slot antenna can support two independent modes, horizontal and vertical polarization modes.

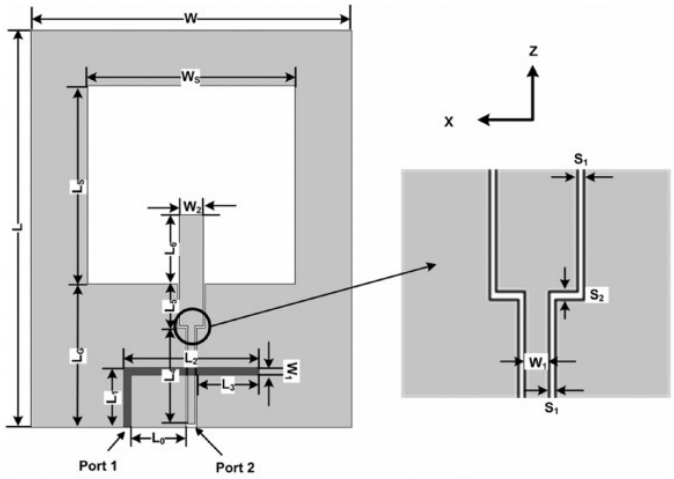


Figure 2-37. Geometry of the proposed CPW antenna [41]. The antenna have two ports which can excite the even and odd modes.

When feeding from Port 1, an odd mode is excited in the CPW structure, which generates a horizontal polarization mode inside the slot. When feeding from port 2, the mode in the CPW is a normal even mode, which can excite a vertical polarization mode inside the slot. The two modes can be observed in Figure 2-38.

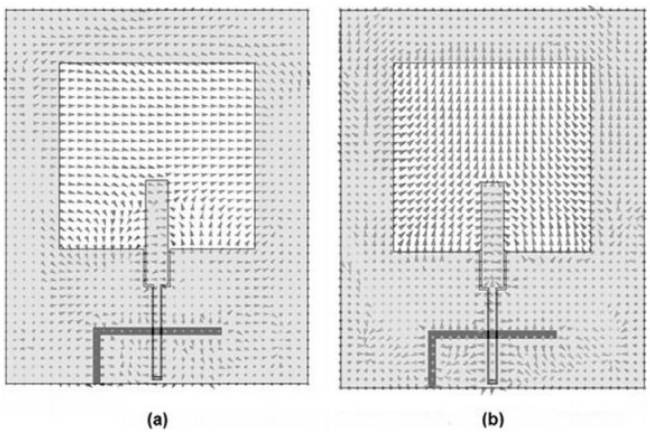


Figure 2-38. Electric field distribution in CPW: (a) odd mode when port 1 is excited and (b) even mode when port 2 is excited [41].

Due to the symmetric and antisymmetric characteristics of the two modes in CPW, high isolation can be achieved between the two ports. Figure 2-39 shows the measured S-parameters of the CPW antenna. The isolation between two ports in the required band is lower than 32.6 dB. The bandwidths of the two ports are all larger than 27.9 %.

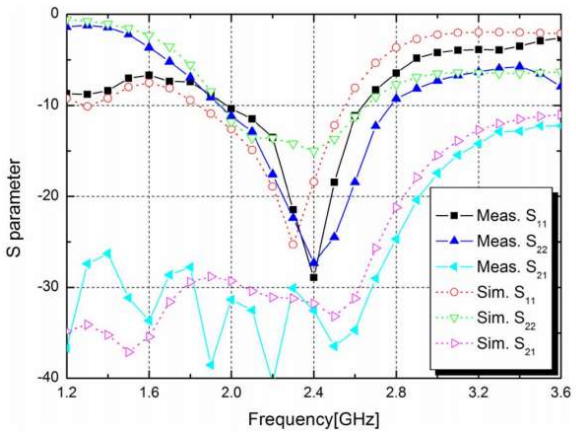


Figure 2-39. Measured and simulated S-parameter of the proposed antenna.

In conclusion, the even mode and odd mode in a CPW structure can be exploited to achieve high isolation, from 20 dB to 30 dB, with a wide bandwidth of more than 23%. However, the isolation level does not meet the isolation requirement in a full-duplex

antenna system. Thus, the CPW must be combined with other isolation techniques to achieve a higher isolation.

2.4.4 Reflective Termination

The works in [46] [72] show that applying a reflective termination in the third port in addition to the two main ports of an antenna system can help to improve the measured isolation from 25 dB to more than 35 dB across the bandwidth. The antenna system, shown in Figure 2-40, has three ports, namely one RX port, one TX port, and one auxiliary port.

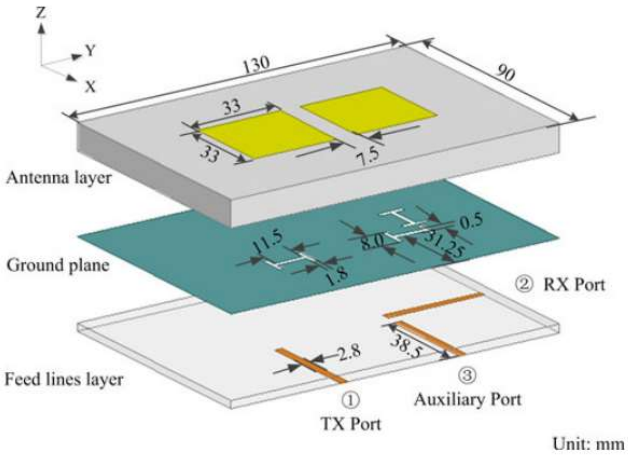


Figure 2-40. Three-dimensional geometry of the aperture-coupled microstrip patch antenna pair with an auxiliary port [46].

The auxiliary port introduces an indirect coupling path, through which the signal is coupled from Port 1 to Port 3 first and then reflected to Port 2. The coupling coefficient C_{21} from Port 1 to Port 2 can be expressed [46] [72] as

$$C_{21} = S_{21} + \frac{S_{23}S_{31}\Gamma_L}{1 - S_{33}\Gamma_L} \tag{2.5}$$

where S_{21}, S_{31}, S_{23}, and S_{33} are the S-parameters of the three-port antenna structure without reflective terminal. Γ_L is the reflection coefficient looking at Port 3. By choosing an appropriate value of Γ_L, C_{21} can be optimized equal or close to zero. The effect of the reflective circuit is shown in Figure 2-41.

Here, the isolation in the simulation of the antenna can be improved from 25 dB to 35-57 dB across the bandwidth by adding a reflective terminal. The measured isolation of the proposed antenna is 35.9 -46.5 dB across 8.76% operating bandwidth.

The work in [72] describes a direct-conversion 45nm SOI CMOS 60 GHz transceiver for same-channel full-duplex applications. A novel polarization-based wideband self-interference cancellation (SIC) technique in the antenna domain is described that can be

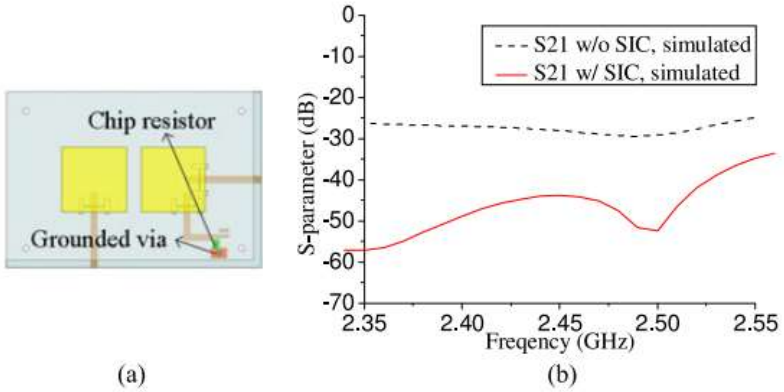


Figure 2-41. (a) Perspective of the antenna pair with the reflective terminal. (b) Simulated S21 of the antenna pair with and without SIC [46]. The SIC improves the isolation from 25 dB to 35-57 dB across bandwidth.

reconfigured from the IC. In order to achieve the high levels of required SIC, a second RF cancellation path from the transmitter output to the LNA output with >30 dB gain control and >360° phase control is also integrated. Antenna and RF cancellation together enable >70 dB of total self-interference suppression even in the presence of nearby reflectors.

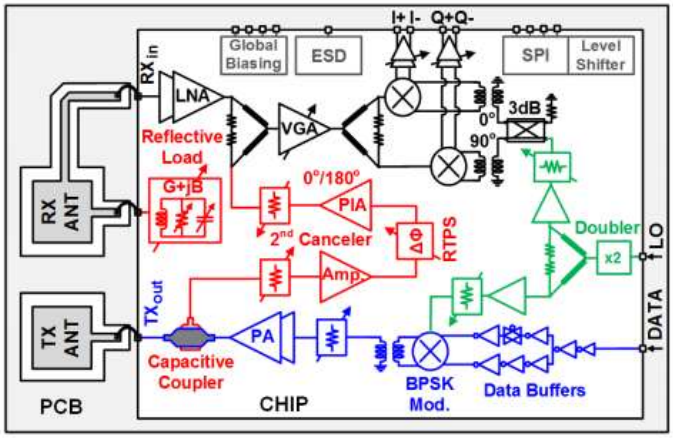


Figure 2-42. Architecture of the full-duplex 60 GHz TX and RX with reconfigurable polarization-based antenna and RF cancellation [72]. The reflective load is to control the reflection coefficient of the auxiliary port in RX antenna to get very low coupling or isolation with TX antenna.

An auxiliary port co-polarized with the transmit port is introduced on the receiver antenna. The auxiliary port creates an indirect coupling path between the transmitter output and the receiver input. It is terminated with a reconfigurable on-chip reflective termination

that reflects the coupled signal in the indirect path to cancel the SI at the receiver input. The coupling coefficient equation is similar to the work in [46] which is calculated by (2.2).

The simulation isolation of the proposed antenna system improves from 30 dB to 50 dB across 8 GHz in simulation.

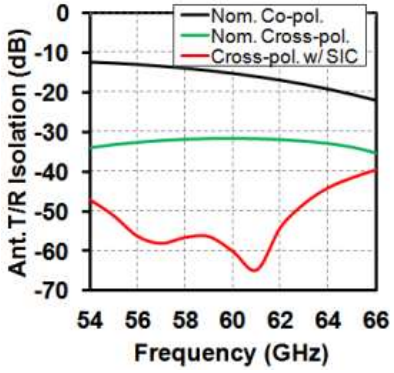


Figure 2-43. The simulation isolation with the SIC using auxiliary port improves from 30 dB to around 50 dB across 8 GHz in simulation [72].

However, the antenna system itself does not have the measured results of isolation and return loss as well as the simulation results. The measured results only exist in the whole IC.

In conclusion, a reflective terminal as an auxiliary port can be applied in a two-port antenna system to achieve high isolation. The antenna system in [72] can get > 50 dB isolation in simulation across a 13% bandwidth. The antenna system in [46] can achieve an isolation of 35.9 dB to 46.5 dB across a 8.76% bandwidth. The isolation level in [46] is not constant across the operating bandwidth due to the mismatch of the reflective terminal at a higher frequency band. This means that the reflective terminal technique can only work for a narrow band system. Moreover, the technique increases the size of the antenna system because of the separated auxiliary port.

2.4.5 Summary

The most important parameter of a full-duplex antenna system is the isolation between two ports of the antenna system. Then, the three isolation techniques, namely coupler, CPW, and reflective termination are reviewed carefully with a focus on the existing issues.

Couplers can be integrated with antennas to improve isolation. The serial configuration can achieve a 50-dB isolation, which is better than the 35-dB isolation in a parallel configuration. However, the integration of the coupler into the antenna normally increases the size of the antenna or increases the number of substrate layers, which does not follow

the current trend of miniaturization or low-cost substrate. Moreover, the high isolation is only maintained in narrow bandwidths.

The even mode and odd mode in a CPW structure can be exploited to achieve a high isolation, from 20 dB to 30 dB, with a wide bandwidth of more than 23%. However, the isolation level does not meet the isolation requirement in a full-duplex antenna system. Thus, the CPW must be combined with other isolation techniques to achieve a higher isolation.

A reflective terminal as an auxiliary port can be applied in a two-port antenna system to achieve a high measured isolation, 35.9 dB to 46.5 dB across a 8.76% bandwidth. However, the isolation level is not constant across the operating bandwidth due to the mismatch of the reflective terminal at a higher frequency band. This means that the reflective terminal technique can only work for a narrow band system. Moreover, the technique increases the size of the antenna system because of the separated auxiliary port.

2.5 Mitigating Activities

Based on the literature review on the adaptive bias technique and the second harmonic short circuit technique, a novel adaptive bias technique, which is driven by the input and output of the PA stage, is proposed in Chapter 3 for a linearity improvement of a CMOS PA at 5.8 GHz. This technique mitigates the existing issues of the reviewed adaptive bias techniques including complex and large schematic and high DC current consumption. In addition, the second harmonic short circuit technique is applied in the PA to improve the P_{1db}.

In Chapter 4, a detailed description is given of the DGS technique which is combined with the stepped slot technique to provide a harmonic suppression capability for the two narrow slot antennas. The proposed combined technique in these two narrow antennas mitigate the problem of the size increment in the previous DGS works. Moreover, the combined technique solves the issue of not having enough suppression at the rejection bandwidth. All of the above advantages come at the expense of a small reduction in operating bandwidth.

The DGS technique can be combined with the high impedance thin microstrip line technique in a novel compact triangle slot antenna, also described in Chapter 4. The combined technique provides a strong out-of-band rejection while attaining a significant reduction in size. Furthermore, the antenna achieves a very wideband with no change in

the radiation gain at 5.8 GHz. This technique which is used in this triangle slot antenna mitigates the existing issues such as size increasement, not having enough suppression at the rejection bandwidth, and a reduction in operating bandwidth.

Finally, in Chapter 5, the reflective termination technique is combined with an even and odd mode isolation in a CPW slot antenna to provide very high isolation between two ports of an IBFD antenna system. The combined technique can achieve much higher isolation than the even & odd mode and the reflective termination technique alone. The proposed antenna has a larger bandwidth compared to that of the coupler technique. Furthermore, the proposed technique mitigates the size increment of the coupler technique.

3 High Linearity CMOS Power Amplifier

Chapter 2 provides a detailed literature review on linearity improvement techniques including adaptive bias techniques and second harmonic short circuit techniques. However, the main limitations of recent adaptive bias techniques are that a typical adaptive bias circuit normally is a complex and large (in terms of area) design in order to convert a small RF signal to the DC bias of the power amplifier. The conventional bias circuit designs, which often include two-stage amplifiers, envelop detectors and envelop shaping circuits, suffer from high complexity, distortion due to a delay through the auxiliary path, extra current consumption, and its large size. This can lead to the degradation of the battery lifetime, which is not acceptable in modern RF transceiver designs with the demand of a longer operating time. These adaptive bias circuits also increase the total size of the PAs considerably, which does not comply with the current trend of miniaturization.

To overcome these limitations, a novel adaptive bias circuit is proposed which utilizes both the output and input signals of a PA. This technique mitigates the existing issues of the reviewed adaptive bias techniques including a complex and large design and high DC current consumption. In addition, the second harmonic short circuit technique is applied in the proposed PA to improve the P_{1db}. The proposed lineariser consumes less than 10 μA RMS current. Furthermore, the size of this auxiliary circuit is very small, which does not add up to the overall size of a PA.

3.1 Introduction

The design of CMOS power amplifiers [73, 74] is mainly challenged by the following factors: Several PA linearization techniques such as adaptive bias circuit [7, 10-14], predistortion shunt-cold FET [15, 16], NMOS diode lineariser [17], and active feedback lineariser (AFL) [48] are considered. Of these, the adaptive bias technique is known for improving linearity efficiently, especially P_{1dB}. However, most of the adaptive circuits use the input signals of PAs, which are small, to control the bias voltages of PA. Therefore, the adaptive bias circuits must use at least two amplifier stages to provide enough gain, leading to the design's complexity, extra current consumption and larger size. For example, the two-diode adaptive bias circuit in [13] consumes a current of up to 6 mA, which is

considerably large for a lineariser. The predistortion shunt cold-FET technique is utilized to improve P_{1dB} by introducing a constant loss at a low power range and reducing the loss at a high-power range, thus, achieving a gain expansion characteristic. [15, 16]. Nevertheless, the shunt cold-FET introduces high insertion losses at low input power due to the large gate width and requires two additional bias sources. The NMOS diode lineariser technique also improves linearity with a simple circuit and small size as the diode can maintain the gate bias level at high input power [17]. However, it does not change the class of PA at high power, thus the improvement in P_{1dB} is limited. The diode techniques can be used in output matching to improve the linearity characteristic [49]. Nevertheless, there is no improvement in P_{1dB} but in intermodulation (IMD) only. Active feedback lineariser techniques can improve linearity by maintaining a constant feedback resistance at low input power and increasing feedback resistance at high input power, hence achieving a gain expansion [48]. The multiple-gated transistor (MGTR) technique, which employs a transconductance cancellation mechanism, requires the high precision of nonlinear cancellation between main and auxiliary paths and thus, higher design complexity [8, 47]. Furthermore, the auxiliary transistors are a considerable size compared to the main transistors, which in turn increase the total size of the PA.

This chapter proposes a novel linear cascode differential CMOS power amplifier which operates at 5.8 GHz ISM, using the low cost TSMC 0.18 μm process technology. The whole PA uses two-stage amplifier topology, the gain-stage (1st stage) and the power-stage (2nd stage) amplifiers, to achieve high gain. The differential topology is utilized in both stages to achieve common noise immunity and eliminate sensitivity to bondwire inductances. To overcome the low break-down voltage problem of the CMOS technology at high power operation, the cascode structure is applied in both stages. Three transmission-line transformers (TLT) are integrated in the whole PA to improve isolation and reduce size compared to conventional transmission line inductors. The novel PMOS lineariser, which works as an adaptive bias circuit in the power-stage, is driven by both the input and the output of the power-stage. The P_{1dB} of the linear PA improves as much as 2.6 dB without degrading the power-added-efficiency (PAE), compared to its conventional counterpart power amplifier in the simulation. With the low voltage supply of 1.8V, the proposed PA delivers a measured output 1- dB compression point OP_{1dB} of 17.5 dBm with the corresponding power-added efficiency ($PAE@P_{1dB}$) of 22.5% at 5.8 GHz carrier frequency. The gain is 18 dB while the reverse isolation is 48.5 dB. The PA has a high figure of merit (*FOM*) with the small silicon die-size of 1.07 mm^2.

3.2 Power Amplifier Design

3.2.1 Design Methodology for RF Power Amplifiers

This section shows how CMOS power amplifier is designed in order to obtain a high-performance power amplifier over specifications. The goal of this research is to design and implement a standalone CMOS power amplifier for easily characterizing S-parameters, P_{1dB}, PAE. The amplifier can also be integrated in a CMOS RF transceiver when needed.

First, the specifications such as operating frequency, S-parameters, power gain, etc. are discussed and described. The technology process, operating frequency and supply voltage are inherited from the current RFID project of our laboratory. From the specifications, the topology of the PA is chosen. Then, the schematic is proposed and simulated in the Synopsys toolkit with the S-parameters of the TLTs extracted from HFSS. In the schematic design process, the transistor size, the matching networks and the TLT size for each stage are determined. To design input and output matching networks in the power amplifier, a two-port network is used in Synopsys. Also, several key design parameters such as the biasing circuit and stability are described. After achieving the specifications in the schematic, the layout is drawn. The post-sim which is for post-layout schematic simulation is implemented. Due to the loss and parasitic of the layout, the results of the post-sim simulation will be different from the schematic simulation. Thus, several rounds of Synopsys simulations are performed again to achieve the given specifications. Since the power amplifier is measured at the board level, it should be packaged to be mounted on the PCB board. The bondwire equivalent models and diagrams are shown in this section to clarify how to incorporate them in simulation.

Then, an RF PCB is developed and built with two surface mount adapter (SMA) ports to measure the power amplifier performance such as S-parameters, current consumption, and output power/input power curve. The stability of the PA can also be observed in the spectrum analyser.

The summary design process used in this dissertation is described in Figure 3-1.

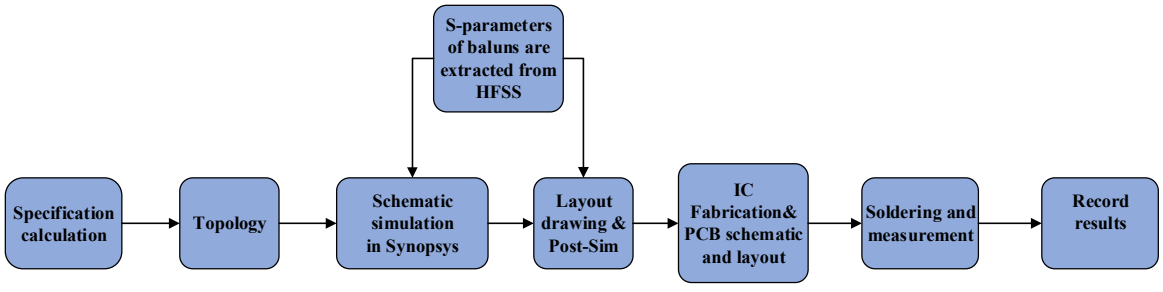


Figure 3-1. Design process of the CMOS Power Amplifier.

3.2.2 Specifications for 5.8 GHz Power Amplifier Design

An RF CMOS power amplifier is designed for our RFID application, which works at 5.8 GHz. The fully integrated differential power amplifier, operating at 5.8 GHz, is implemented in the 0.18 μm TSMC 20K2f process. This process has six metal layers with an ultra-thick layer of 23400 Angstrom (20K) on the top layer M6. The MIM capacitor in this process has 2 femtofarad (2fF) per μm^2. The specific key design requirements are listed in Table 3-1. The generic specifications namely supply voltage, operating frequency, and the CMOS process are taken from the general specification of our industrial grade RFID project. The latest challenges presented in the literature lead us to choose the specific design requirements, namely power gain, output power P_{1dB}, and power added efficiency PAE.

Table 3-1. Design specifications of the 5.8 GHz power amplifier

Design Parameters	**Specification**
CMOS process (μm)	0.18
Supply voltage (V)	1.8
Operating frequency (GHz)	5.7 to 5.9
Power Gain S_{21}(dB)	>15
Output Power (P_{1dB}) (dBm)	>18
PAE @P_{1dB} (%)	>20
S_{11} and S_{22}	>10 dB
Stability	No Oscillation

3.2.3 Power Amplifier Topology

This section describes the background theory of the two-stage design, in which both the gain-stage and the power-stage are biased to work at class B. The topology has the advantages of low quiescent current, high efficiency, and especially high P_{1dB} compared to a single stage design. Then, the benefits of the differential topology, namely noise immunity, less sensitivity to bondwire inductances, and a close-to-zero second harmonic component, are discussed in the next section. After this, the working principles of the cascode structure in both the gain-stage and the power-stage with RC feedback to avoid break down voltage and improve stability & bandwidth are explained in detail.

Based on the specifications of the previous section, the two-stage topology of the conventional power amplifier is proposed in Figure 3-2. The conventional two-stage topology comprise two normal stage amplifiers and matching LC networks, without any specific technique to improve linearity or efficiency. Then, the linear power amplifier with the PMOS lineariser is proposed in Figure 3-3. The topology of the linear power amplifier is similar to the conventional power amplifier except the two PMOS linearisers, which are connected to the input and output of the PA stage.

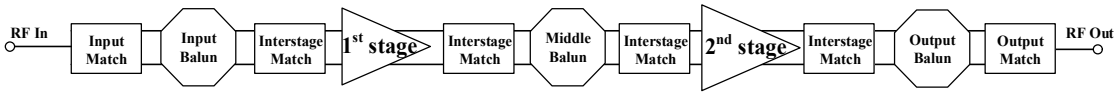


Figure 3-2. The conventional two-stage power amplifier with matching networks.

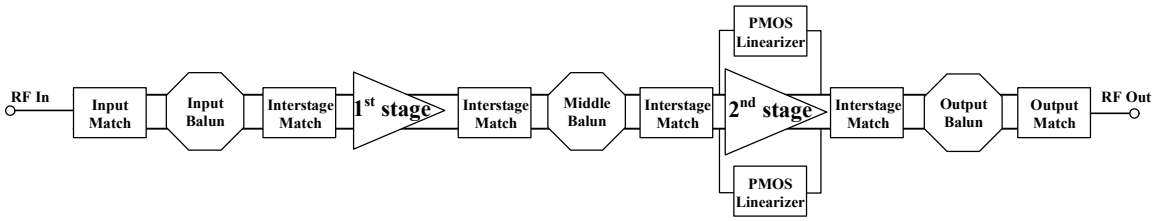


Figure 3-3. The linear power amplifier with PMOS linearisers.

The two-stage topology is chosen to provide the required gain shown in Table 3-1, since the one-stage amplifier can supply a maximum 10 dB gain [75]. The power-stage or the 2nd stage is designed to provide maximum output power whereas the gain-stage or the 1st stage is designed for maximum gain. The bias voltages of both the stages are optimized in consideration of high P_{1dB} while maintaining the moderate power gain of more than the design specification of 15 dB. The design procedure starts from the output of the PA since it has a strong influence on the output power and efficiency of the whole power amplifier.

A differential structure is chosen in the proposed design due to its noise immunity, less sensitivity to bondwire inductances, and close to zero second harmonic component, which is explained in the next section. Since the differential power amplifier still needs a single-ended input and provides a single-ended output, one port of the input TLT and output TLT is shorted to ground to convert single-ended signals to differential signals and vice versa.

A cascode common-source common-gate configuration is used in both the 1st stage and the 2nd stage to avoid the low break-down voltage problem of CMOS technology and provide higher isolation between the input and output in each stage. The explanation of the benefits of a cascode structure is given in detail in the next section. The RC feedback

topology is used with the cascode configuration to improve stability, linearity and bandwidth.

The two PMOS linearisers are connected to the input and output of the 2nd stage to improve P_{1dB}, which is shown Figure 3-3. The working principle of the PMOS linearisers are derived using the Kirchhoff's current and voltage laws in the next section.

3.2.3.1 Two-Stage Design

The gain-stage or the 1st stage is biased at class B to maintain a low quiescent current but still supply enough gain. The power-stage or the 2nd stage is also biased at near the threshold voltage or class B to have a low quiescent current also. Because the 2nd stage has the most influence on the quiescent current and efficiency of the whole PA, and the class B amplifier has a low quiescent current and high efficiency, the whole PA will have the advantage of a low quiescent current and high efficiency. However, the class B amplifier normally has a low linearity due to distortion at the zero-crossing point, leading to the low linearity of the whole PA. Fortunately, this low linearity of the power-stage working as a class B amplifier can be compensated by optimizing the bias point of the gain-stage, as proven below.

The cascaded combination shown in Figure 3-4 of the two-stage amplifiers is also well known to increase linearity [11, 76].

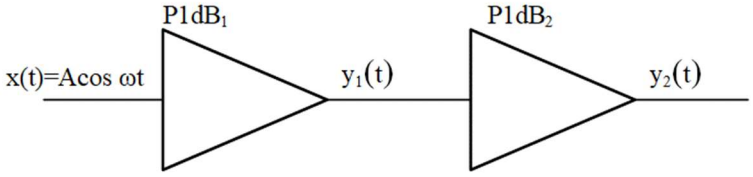


Figure 3-4. The cascaded combination of a class A and class B amplifiers to improve linearity. $Acos(wt)$ is the input signal fed to the amplifier 1 [11, 76].

The output $y_1(t)$ and $y_2(t)$ can be expressed as follows:

$$y_1(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t)$$

$$y_2(t) = \beta_1 x(t) + \beta_2 x^2(t) + \beta_3 x^3(t) \quad (3.1)$$

where $\alpha_1, \alpha_2,$ and α_3 are the coefficients of the input/output characteristic of amplifier 1 in Figure 3-4. $\beta_1, \beta_2,$ and β_3 are the coefficients of the input/output characteristic of amplifier 2 in Figure 3-4. x(t) is the input signal fed to amplifier 1.

Then

$$\begin{aligned} y_2(t) &= \beta_1\left(\alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t)\right) \\ &+ \beta_2(\alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t))^2 \\ &+ \beta_3(\alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t))^3 \end{aligned} \tag{3.2}$$

Consider only the first and third order terms, with $x(t) = Acos(\omega t)$

$$\begin{aligned} y_2(t) &= \beta_1\alpha_1 x(t) + \quad (\alpha_3\beta_1 + 2\alpha_1\alpha_2\beta_2 + {\alpha_1}^3\beta_3)x^3(t) \\ &= \quad \left(\beta_1\alpha_1 A + \frac{3(\alpha_3\beta_1 + 2\alpha_1\alpha_2\beta_2 + {\alpha_1}^3\beta_3)A^2}{4}\right) cos\,(\omega t) \end{aligned} \tag{3.3}$$

The P_{1dB} is calculated, when the power gain, which is equal to $\beta_1\alpha_1 A + \frac{3(\alpha_3\beta_1+2\alpha_1\alpha_2\beta_2+{\alpha_1}^3\beta_3){A_{in,1dB}}^2}{4}$, drops 1 dB from its constant value, $\beta_1\alpha_1$.

Hence

$$\begin{aligned} &20log\left|\beta_1\alpha_1 A + \frac{3(\alpha_3\beta_1 + 2\alpha_1\alpha_2\beta_2 + {\alpha_1}^3\beta_3){A_{in,1dB}}^2}{4}\right| \\ &= 20log|\beta_1\alpha_1| - 1dB \end{aligned} \tag{3.4}$$

Therefore, the equation to calculate the input P_{1dB} of the whole PA is expressed as follows:

$$A_{in,1d} = \sqrt{0.145\left|\frac{1}{\frac{\alpha_3}{\alpha_1} + 2\alpha_2\frac{\beta_2}{\beta_1} + \alpha_1^2\frac{\beta_3}{\beta_1}}\right|} \tag{3.5}$$

where $\alpha_1, \alpha_2, \alpha_3, \beta_1, \beta_2$ and β_3 are the first, second and third order of non-linear system $y_1(t)$ and $y_2(t)$, respectively. $A_{in,1dB}$ is the input P_{1dB} of the whole PA. In an ideal differential structure, the second order α_2 and β_2 are equal to zero [77]. Here, in the gain-compression system, $\frac{\alpha_3}{\alpha_1} < 0$, and in the gain-expansion system, $\frac{\beta_3}{\beta_1} > 0$ [78]. Therefore, with an appropriate selection of $\alpha_1, \alpha_3, \beta_1$and β_3, $A_{in,1dB}$ of a two-stage topology can be improved compared to that of a single stage, which is $A_{in,1d} = \sqrt{0.145\frac{\alpha_1}{\alpha_3}}$.

However, in a practical differential structure, the mismatches of the differential pairs, the non-linear gate-source capacitance C_{gs}, the non-linear transconductance, and other parasitic components generate the second harmonic, which here is α_2 and β_2. Therefore,

the second harmonic short circuit technique is employed at the common nodes of the CG and the CS transistors of both the gain-stage and power-stage to reduce this second harmonic component [6] [53].

The final bias voltage of the gain-stage is 0.63V whereas that of the power-stage or the PA stage is 0.54V in the proposed design. This combination can ensure that the whole PA has a low quiescent current and high efficiency with moderate linearity or P_{1dB}. The P_{1dB} can then be further improved using a novel PMOS linearity circuit, which is an adaptive bias circuit. The PMOS linearity circuit increases the bias voltage, thus changing the working class of the power-stage to near class A.

3.2.3.2 Differential Topology

A differential topology, shown in Figure 3-2, is chosen in the proposed design due to its noise immunity, less sensitivity to bondwire inductances, and close to zero the second harmonic component. This section provides a detailed explanation of these beneficial characteristics.

A differential signal is one that is measured between two nodes that have an equal and opposite signal around a fixed voltage. The two nodes should have equal impedance to this potential. The centre potential in differential signalling is called the “common-node” (CM) level, which is usually equal to 0 V.

The differential signal has a proficient advantage over the single-ended signal, that is a higher immunity to environmental noise. The principle of this operation can be seen in Figure 3-5 [79] .

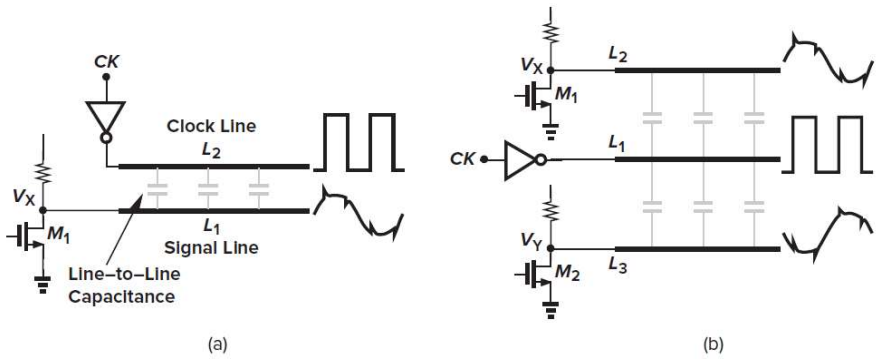


Figure 3-5. (a) Degradation of a signal due to coupling to a clock line; (b) Coupling reduction due to differential operation [79].

Figure 3-5(a) shows what happens when a large clock line is placed near a sensitive and small signal line. At each transition of the clock signal, the quality of the signal on line

L_1 is corrupted due to capacitive coupling between the lines. This issue can be mitigated by using the differential operation in Figure 3-5(b). In this operation, the sensitive signals in line L_2 and L_3 have the same amplitude of corruption but in the opposite phase. Therefore, when the two signal lines are combined (added), the differential output is not corrupted (noises are eliminated as they are present in both signals). That is, the differential system has the capability to reject common-node noise.

Another advantage of differential PAs over single-ended PAs is that the former can alleviate the very large transient currents that is pulled from the supply to the ground. The concept is described in Figure 3-6 [75].

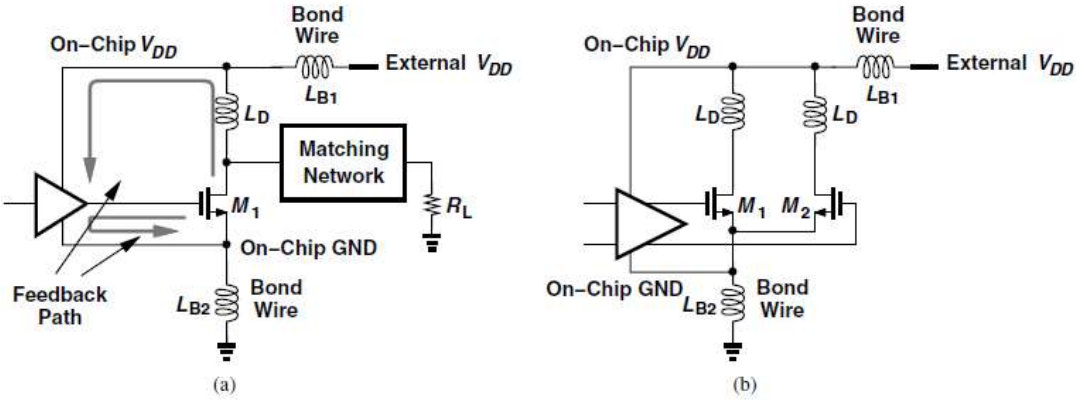


Figure 3-6. (a) Feedback in a single-ended PA due to bond wires, (b) less problematic situation in a differential PA [75].

In Figure 3-6(a), if the supply bondwire inductance L_{B1} and L_{B2} are comparable with the L_D, they will alter the impedance or resonance properties of the output network. Furthermore, they will allow some of the output signal to travel back to the preceding stage through the V_{DD} line, causing a ripple in the frequency response or instability. In Figure 3-6(b), the differential topology restricts the transient current from V_{DD} and ground lines due to the virtual ground forming at those common nodes (V_{DD} and ground). This means that the topology is less sensitive to L_{B1} and L_{B2}.

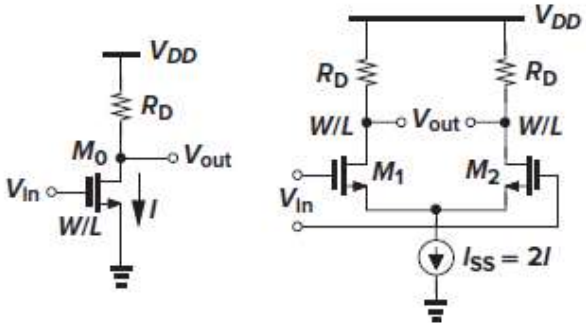


Figure 3-7. Single-ended and differential amplifier with same voltage gain [79].

The differential circuits exhibit an odd-symmetric input/output system, i.e. f(-x)=-f(x). This can be proven by analysing the current of the single-ended and differential amplifiers in Figure 3-7 [79].

The drain current of the single-ended amplifier is expressed as follows [79]:

$$I_{D0} = I + \mu_n C_{ox} \frac{w}{L}(V_{GS} - V_{TH})V_m cos(\omega t) + \frac{1}{4}\mu_n C_{ox} \frac{w}{L} V_m^2[1 + cos(2\omega t)] \quad (3.6)$$

The drain current of the differential amplifier is expressed as follows [79]:

$$I_{D1} - I_{D2} = I + g_m \left[V_m - \frac{3V_m^3}{32(V_{GS} - V_{TH})}\right] cos(\omega t) \quad - g_m \frac{V_m^3 cos(3\omega t)}{32(V_{GS} - V_{TH})^2} \quad (3.7)$$

where g_m is the transconductance of transistor, $V_m cos(\omega t)$ is the signal applied to each circuit in Figure 3-7. V_{GS} is the voltage between gate (G) and source(S) of transistor. V_{TH} is the threshold voltage. W is the width of transistor and L is the length. $\mu_n C_{ox}$ is the constant of the technology.

A comparison of equations (3.6) and (3.7) indicates that the differential circuit does not have the second harmonic component. Furthermore, the third harmonic component is also much smaller than the second harmonic components of the single-ended counterpart, for example, if $V_m = 0.2(V_{GS} - V_{TH})$, (3.7) yields a distortion of 0.125%, which is smaller than 5% of (3.6).

3.2.3.3 Cascode Amplifier Stage

The cascode stage is used within the differential topology in the proposed design to avoid the low break-down voltage problem of CMOS technology and provide isolation between input and output. The basic cascode configuration is shown in Figure 3-8 [75].

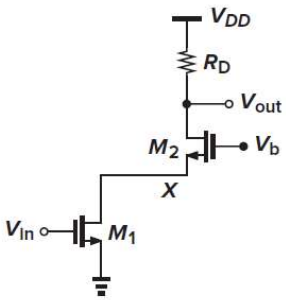


Figure 3-8. Basic Cascode Configuration [75].

A small signal drain current generated by transistor M_1 is driven proportionally with the small signal input voltage, V_{in}. This current is routed by the transistor M_2 to R_D. The M_1 is called the input device and the M_2 is called the cascode devices. The bias conditions of the cascode where M_1 and M_2 operate in saturation is as follows [79]:

$$V_{out} \geq (V_{GS1} - V_{TH1}) + (V_{GS2} - V_{TH2}) \tag{3.8}$$

The minimal output level for which both transistors operate in saturation is equal to the overdrive voltage of M_1 plus that of M_2. That is to say, M_2 reduces the output voltage swing by at least the overdrive voltage of M_2. The input-output characteristics of a cascode stage is shown in Figure 3-9 :

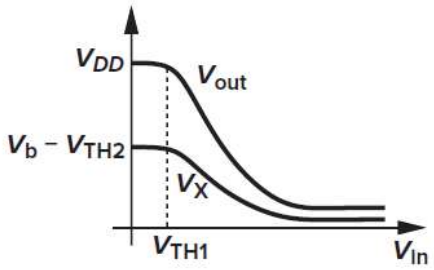


Figure 3-9. Input-output characteristics of a cascode stage [75].

As can be seen, the maximum voltage swing of the transistor M_1 is the $V_b - V_{TH}$. Here, in the proposed design, the nominal supply voltage of the process is 1.8V and the threshold voltage is approximately 0.5V. The V_b of both the 1st stage and the 2nd stage amplifiers are connected to the 1.8V, as shown in Figure 3-10. Therefore, the maximum voltage of the M_1 is 1.3V.

The drain waveform of the cascode stage is described in [75].

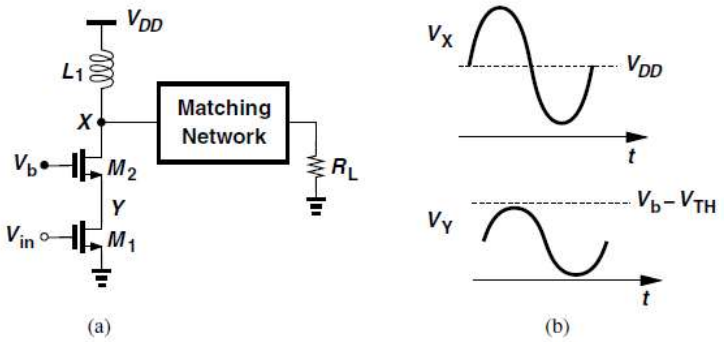


Figure 3-10. (a) Cascode PA and(b) its waveforms [75]. Both V_X -V_b and V_Y are smaller than V_{DD}.

As can be seen, the voltage V_X -V_b (when V_b is set equal to V_{DD}) and V_Y are both smaller than V_{DD}.

RC Feedback Design

RC feedback networks, which comprise a series resistor and a series capacitor, are placed between the drain of the common gate (CG) transistor and the gate of the common source (CS) transistor of both the gain-stage and power-stage, as shown in Figure 3-11.

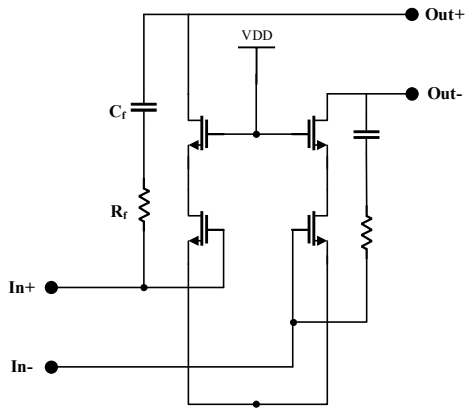


Figure 3-11. RC feedback network, including R_f and C_f, using with cascode configuration.

The block diagram of the RC feedback can be seen in Figure 3-12.

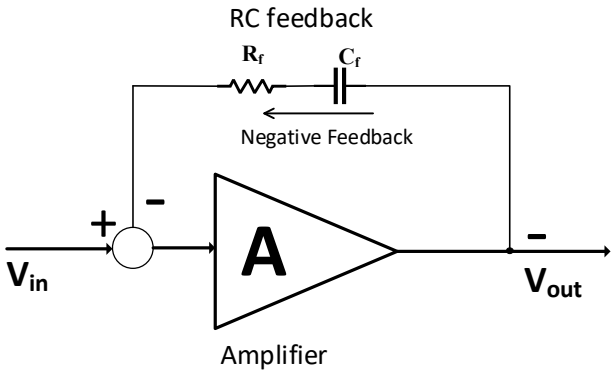


Figure 3-12. Negative feedback concept for a general amplifier [50] [75]. A is the gain of the amplifier.

$$\frac{\text{Vout}}{\text{Vin}} = \frac{A}{1 + \beta A} \tag{3.9}$$

$$\beta = \frac{Zin}{Zin + \sqrt{R_f^2 + \left(\frac{1}{j\omega c_f}\right)^2}}$$

where Z_{in} is the input impedance at V_{in}, A is the gain of the amplifier in Figure 3-12.

From (3.9), it can be seen that the overall gain drops by (1+βA). However, when A is large enough, βA>>1, the overall gain is equal to 1/β. This means that the closed-loop gain is less sensitive to device parameters and frequency than the open-loop gain. Therefore, it can be said that negative feedback stabilizes the gain and improves the operating bandwidth.

The RC feedback can provide another freedom of choice to control the stability of the amplifier by means of improving stability K factor in exchange of gain.

The values of R and C are optimized based on the gain value, input and output return loss, and stability factor K.

3.2.4 Power Amplifier Schematic

This section describes the detailed schematic of the proposed PA. The design process of the schematic in the Synopsys simulation is represented in block diagrams.

Next, the improvement of the saturation output power and P_{1dB} using the second harmonic short circuit technique is clarified using a comparison of the power transfer curves with and without the circuits. The HFSS simulation of three on-chip transmission-line transformers are described in detail in the next section. The parameters of a TLT such as coupling factor K, quality factor Q, surface resistance R, and inductance L at 5.8 GHz are extracted from the S-parameters using Synopsys. The DC current capability of TLTs or the minimum trace width of the middle TLT and output TLT are calculated to make sure that the whole PA can work in the highest current, thus the output power condition.

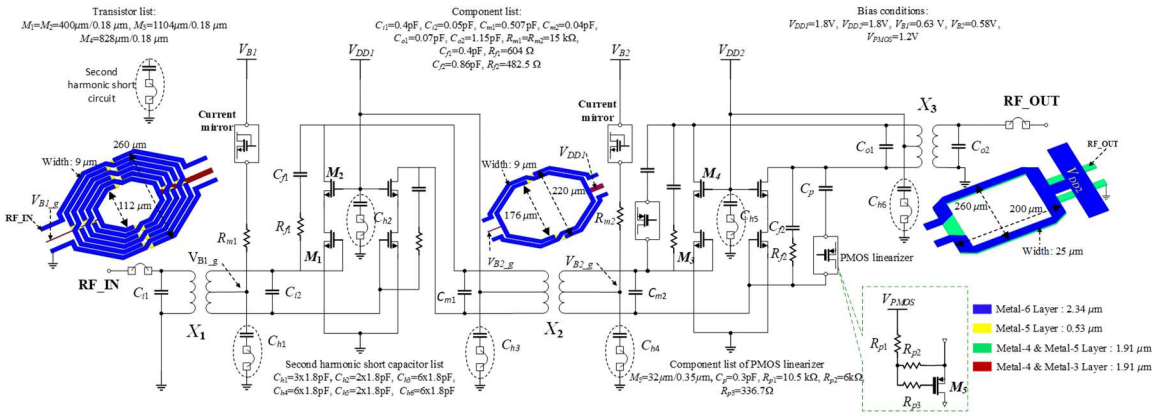


Figure 3-13. The linear PA schematic with PMOS linearisers.

Then, the linearization with the PMOS Adaptive Bias Circuit section explains the working principle of the PMOS lineariser. The two PMOS linearisers are placed between the input and output of the PA stage to improve the P_{1dB} of the whole power amplifier. The Kirchhoff's current and voltage laws are used to derive the relationship between the bias

voltage of the PA stage with other electrical parameters of the whole PA and the PMOS lineariser.

Figure 3-13 shows the schematic of the proposed PA consisting of two stages. The 1st stage serves as the gain-stage amplifier, while the 2nd stage is the power-stage amplifier. Each stage adopts pseudo-differential cascode topology in which common source transistors (M_1, M_3) are cascaded with common gate transistors (M_2, M_4).

The values of C_{i1}, C_{i2}, and C_{o1}, C_{o2} are chosen for the input and the output matching with 50 Ω at 5.8 GHz. The values of C_{m1} and C_{m2} are optimized for interstate matching between the 1st and the 2nd stage amplifiers.

RC feedback networks, R_{f1}, C_{f1} and R_{f2}, C_{f2}, are deployed between the drain of M_2/M_4 and the gate of M_1/M_3, respectively, as shown in Figure 3-13. These negative feedback networks are used to improve the stability, linearity and bandwidth of the PA with the expense of negligible gain reduction [10].

As seen in Figure 3-13, large capacitors from C_{h1} to C_{h6} are employed at virtual grounds of all three transmission-line transformers (TLTs: X_1, X_2 and X_3) and the gates of M_2 and M_4 to provide ac-ground short for the even-order unwanted harmonics [6, 53].

R_{m1} and R_{m2}, chosen as 15 kΩ, are used to block the RF signal leaking into the bias voltage supply V_{B1} and V_{B2}.

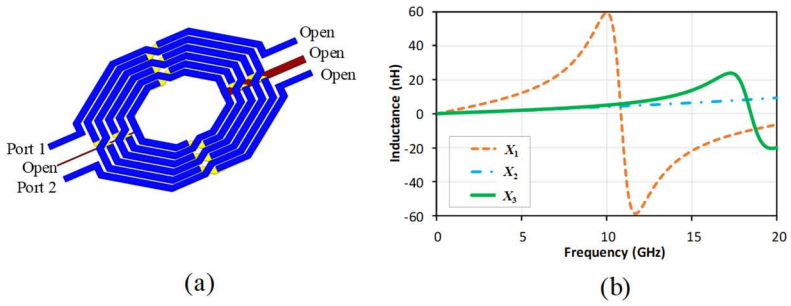


Figure 3-14. Simulated inductance of transformers. (a) Simulation setup. (b) Self-resonance frequencies (inductance=0) >> 5.8 GHz.

The three TLTs are integrated in the PA, as seen in the Figure 3-13. The centre taps of these transformers are used to apply bias and supply voltages. X_1 and X_2 are chosen as conventional hexagonal TLTs with an interleave type to reduce complexity in the design process. X_3 is the overlay type to achieve a high coupling factor in order to minimize the insertion loss of the output matching network [80]. X_3 is implemented in the top three metals with widths of 25 µm to withstand the high current of the 2nd stage. The simulated

maximum available gain (MAG) or minimum insertion loss $\left(n_{MAX} = 10^{MAG/10}\right)$ of X_3 is 1.46 dB and simulated coupling factor k is 0.8, which are in a reasonable range for an on-chip overlay TLT [80]. The TLTs' radiuses and number of turns are chosen to ensure the self-resonant frequencies of the three TLTs are much higher than the operating frequency 5.8 GHz, as shown in Figure 3-14. As a result, the inductance values of the TLTs do not vary too much from the designed values due to process variations in the fabrication prototype.

The bias voltage V_{B1} of the 1st stage is 0.63V while V_{B2} of the 2nd stage is 0.58V. These bias voltages are chosen to be slightly higher than the threshold voltage of the nMOS transistors to achieve a low quiescent current and the high efficiency of the class B amplifiers.

The transistors' lengths are all 0.18 μm while the widths are varied among the transistors to optimize the PA's performance. The widths of M_1 and M_2 of the 1st stage are both 400 μm.

They are chosen such that the overall gain of the proposed PA is met. However, the width ratio of M_3 and M_4 of the 2nd stage is chosen as 4:3 (M_3:M_4) while considering the linearity of the PA. The width of M_4 (828 μm) is chosen smaller than M_3's (1104 μm) to lower its output capacitance to avoid degrading the output matching network's Q-factor [81]. The width of M_3 is chosen to provide enough gain for the PA.

The Synopsys simulation is carried out based on the design process described in Figure 3-15. The output return loss is a good beginning of the design process because it is the most sensitive parameter to the saturation power and P_{1dB} (both P_{1dB} and P_{SAT} are at measured at

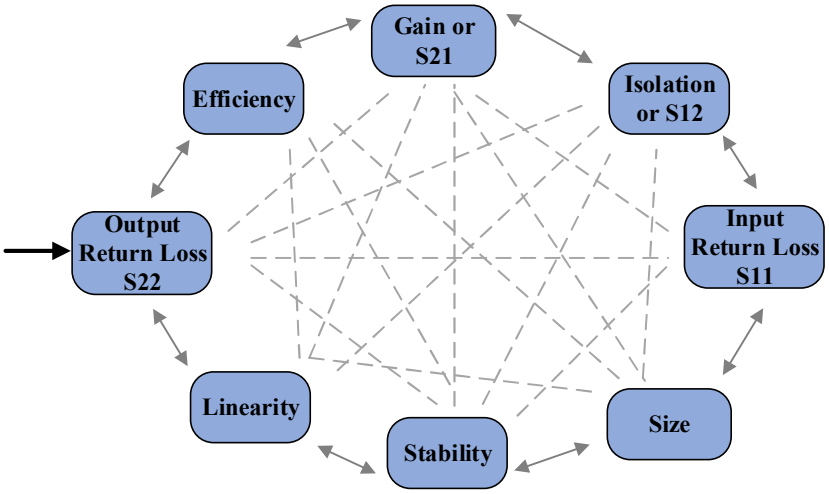


Figure 3-15. Optimization process of the conventional and linearity PA schematics and layouts in Synopsys. The schematic optimization process does not have the parameter "Size".

the output). The input return loss is also less sensitive to the change in the output return loss because of the high reverse isolation, S_{12}, from the output to input. Then, during the optimization process, the parameters such as input/output return loss, efficiency, isolation, stability, and size (in layout optimization process) must be considered together because they are intertwined.

After the schematic of the conventional PA is designed, the PMOS linearisers are put in the PA stage. The conventional PA is designed with the saturation power or P_{SAT} equal or larger than 18 dBm because the P_{1dB} of the linearity PA will be close or equal to the P_{SAT} , as shown in Figure 3-16. After the PMOS linearisers are put in, all the parameters in Figure 3-15 are changed. Then, several optimization processes are repeated following Figure 3-15 to achieve the desired specifications described in Table 3-1.

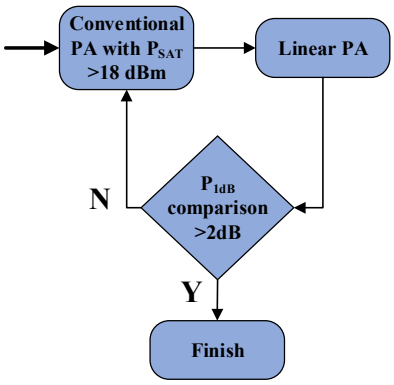


Figure 3-16. Design process of the linear PA schematic.

3.2.4.1 Second Harmonic Short Circuit

In the proposed designs, the second harmonic short circuit technique is applied to improve the P_{1dB} and saturation power.

The second harmonic short circuits are depicted in the Figure 3-13 in the dash ellipse. There is a total of six second harmonic short circuits in this design. The circuits are composed of big MIM capacitors, C_{h1} to C_{h6}, and combined inductors of ground-bonding wires and transformers, which is designed to resonate at the second harmonic frequency. These circuits eliminate the second harmonic components of the whole PA, thus improving the linearity of the whole PA as discussed in detail in Chapter 2 of this dissertation. In addition, the working principle of these circuits can be explained using equation (3.5). These circuits terminate the second harmonic components, here α_2 and β_2, thus improving $A_{in,1dB}$ (3.5).

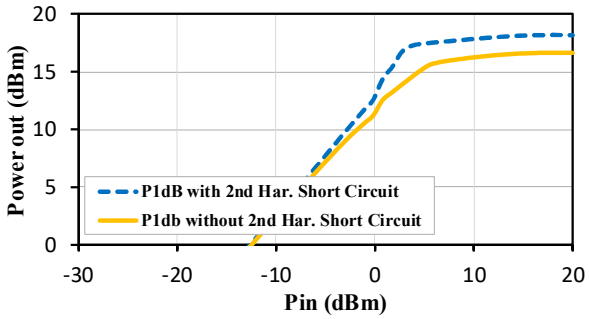


Figure 3-17. Comparison between P_{1dB} curves, with and without 2nd short harmonic circuit.

Figure 3-17 compares the P_{1dB} curves with and without the second harmonic short circuit at the output TLT, which is the circuit most sensitive to the linearity improvement of the PA (the second harmonic at the output is the largest due to the large size of the PA transistors, which have a large non-linear parasitic such as gate-source capacitor C_{GS} and drain-source capacitor C_{DS}). The circuit improves saturation power 1.5 dB, from 16.7 dBm to 18.2 dBm, as seen in Figure 3-17. The P_{1dB} improves 7.61 dB from 9.79 dBm to 17.4 dBm. This circuit is connected at the common ground at the middle of the output balun, as shown in Figure 3-13. The value of the MIM cap is 10.8 pF, which is chosen based on Harmonic Balance Simulation in Synopsys software. Other second harmonic short circuits are chosen to have the same value of the MIM cap.

3.2.4.2 On-Chip Transmission Line Transformer (TLT) Design

The use of on-chip transformers prevents the degradation of the circuit performance due to the loss and the parasitic from the chip interface. Moreover, the integration with on-chip TLTs can greatly reduce the size of the RF transceivers, although on-chip TLTs suffer from a low-quality factor Q and high isolation loss. This leads to performance degradation in noise, gain, output power, and power consumption. However, the advantages overcome the disadvantages [82]. Therefore, the three transmission-line transformers (TLTs) are integrated in the whole PA, as shown in Figure 3-13, which are input, middle and output TLTs. The three TLTs are simulated with a 3D electromagnetic simulation software, ANSYS HFSS. The next three sections explain the working principles of the TLTs, as well as the HFSS setup and simulation. In addition, the current handling capability of these TLTs is calculated based on their geometric parameters.

Background of On-Chip TLTs

Baluns or transformers have been used in radio frequency (RF) and microwave circuits from the early days of telegraphy [80]. The operation of a passive transformer is based on

the mutual inductance between two or more conductors or windings. In addition, DC current can be blocked by the transformer, allowing the two coils to be biased at two different voltages.

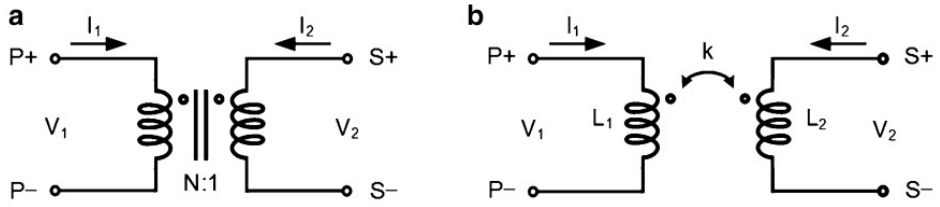


Figure 3-18. Schematic symbol of (a) an ideal N : 1 transformer and (b) a transformer made of two coupled inductors [82].

Figure 3-18 shows the schematic symbol of ideal transformers [82]. In Figure 3-18(a), $N=V_1/V_2$ is the turn ratio between the primary coil (P+ and P-) and the secondary coil (S+ and S-). The impedance of the primary coil is equal to N^2 of the impedance of the secondary coil. Figure 3-18(b) shows the transformer of the two coupled inductors. The relationship between the voltages and currents of the ideal transformer can be described as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} sL_1 & sM \\ sM & sL_2 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \tag{3.10}$$

where $M=-(d\phi_{12} / dI_1)=-(d\phi_{21}/dI_2)$, ϕ_{12} and ϕ_{21} is the magnetic fluxes in the primary and secondary coil generated by the current I_1 and I_2 in its neighbouring coil. L_1 and L_2 are the inductance of the primary coil and the secondary coil, respectively.

The magnetic coupling coefficient k defined as the ratio between mutual inductance and self-inductance is as follows:

$$k = \frac{M}{\sqrt{L_1 L2}} \tag{3.11}$$

There is no leakage of magnetic flux or conductor loss in an ideal transformer, so k is equal to unity. However, in the case of an integrated transformer, the coupling coefficient is always less than one due to lossy substrate, which has a poor confinement of magnetic flux.

The transformer symbols with different coupling directions are described in Figure 3-19.

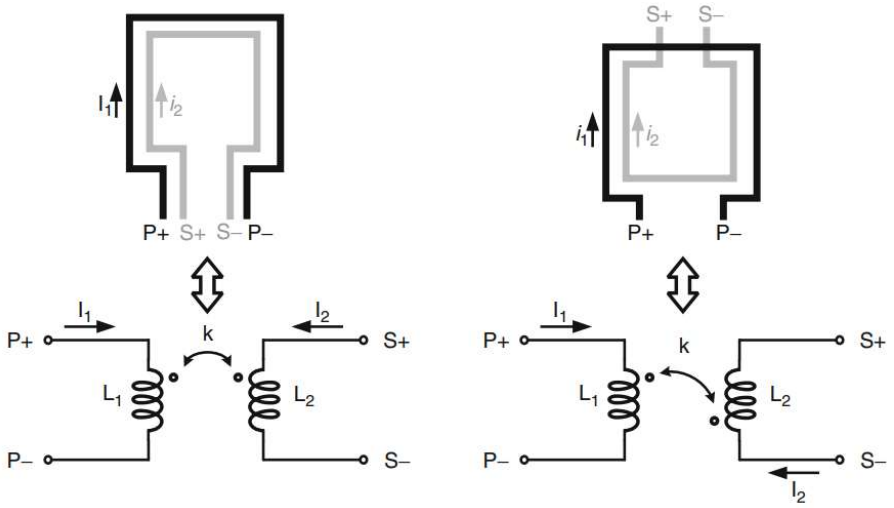


Figure 3-19. Transformer with different coupling directions and the schematic symbols [82] [80].

The transformer layout can be an interleaved, taped, or stacked layout, as shown in Figure 3-20.

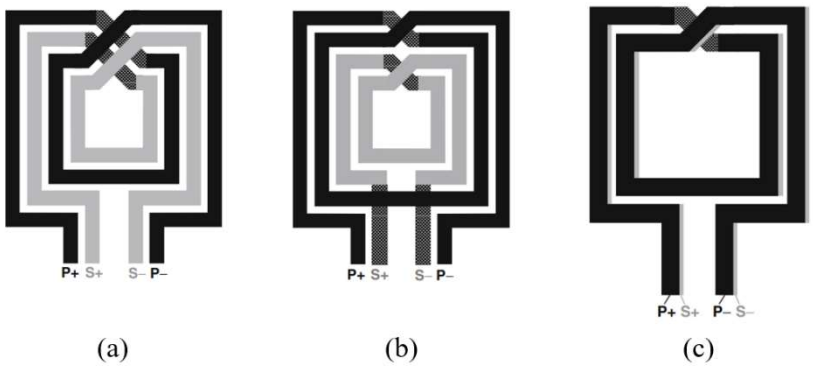


Figure 3-20. Three layout types of on-chip transformers. (a) Interleaved type, (b) Taped type, and (c) stacked layout.

In the interleaved transformer in Figure 3-20, both the primary and secondary coils are implemented with the same metal layer. The thick top layer, which is several times thicker than the other metal layers, is used for maximum quality factor Q and high self-resonant frequency.

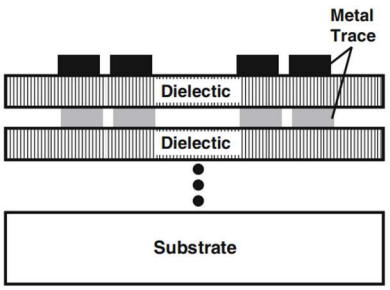


Figure 3-21. Cross-section view of a CMOS process [82] [80].

The distance of the top layer to the low resistance substrate in the CMOS process is also much higher, thus reducing the loss to the substrate. The lower metal layers can be used as bridges at the cross-over point. In a taped transformer, both coils are fabricated in the top metal layers, as seen in Figure 3-20. In the stacked transformer layout in Figure 3-21, the primary and secondary coils are fabricated in different metal layers. The vertical coupling is utilized to provide maximum magnetic coupling, because the dielectric thickness is much smaller than the minimum space between the two neighbouring top metal traces. As a result, the inter-coil capacitance increases due to the small dielectric thickness, leading to small self-resonance frequency.

The performance of different types of on-chip transformers is compared in Table 3-2.

Table 3-2. Comparison of different types of on-chip transformers [82] [80].

Transformer structure	k	Self-inductance	Area	Self-resonant frequency
Interleaved	>0.7	Medium	Medium	Medium
Tapped	0.3–0.7	Low	Large	High
Stacked	~0.9	High	Small	Low

As shown, the interleaved transformer has a moderate k coefficient while the stacked transformer has the highest. However, the self-resonant frequency shows an opposite trend.

HFSS Simulation of the Three TLTs

The input TLT or input balun in HFSS is described in Figure 3-22. A hexagonal shape for the TLT is chosen to reduce the overall area. The type of the TLT is interleaved, which is similar to Figure 3-20. The TLT on the right of Figure 3-22 is the rotation of the one on the left for 3D viewing. The red metallic rectangular surrounding the TLT is the place where the simulation current can return, following the setup instructions in HFSS. It also represents the metallic ground formed by metallic filters using in the layout. The coupling direction of the TLT is described on the right of Figure 3-19. The V_b narrow transmission line connected to the centre of the trace of the secondary coil is S+ and S- and can be used to supply DC bias voltage to the gain-stage. A very small value of 2um is chosen for the width of this V_b because the bias current is close to zero. The V_{DD} wide transmission line is used to supply DC supply voltage but is not utilized in the input stage. The width of the V_{DD} line is chosen to be 1.5 times the width of the coil in order to handle a large DC current.

The input TLT is used to convert a single input RF signal to the differential output, which is, in turn, connected to the differential input of the gain-stage. It also provides an inductance value for the input impedance matching circuit. Because the TLT is composed

of two separated coils, the decoupling capacitors on the signal line of the input of the gain-stage can be omitted, thus reducing space.

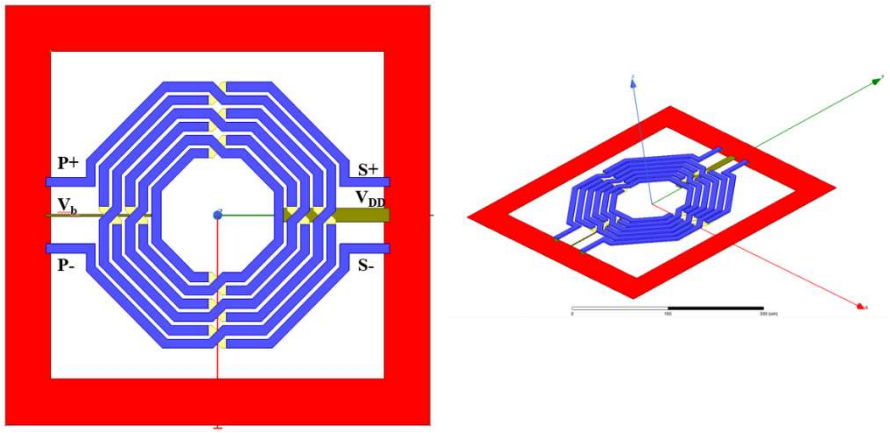


Figure 3-22. HFSS simulation setup of input TLT from a front view and 3D view.

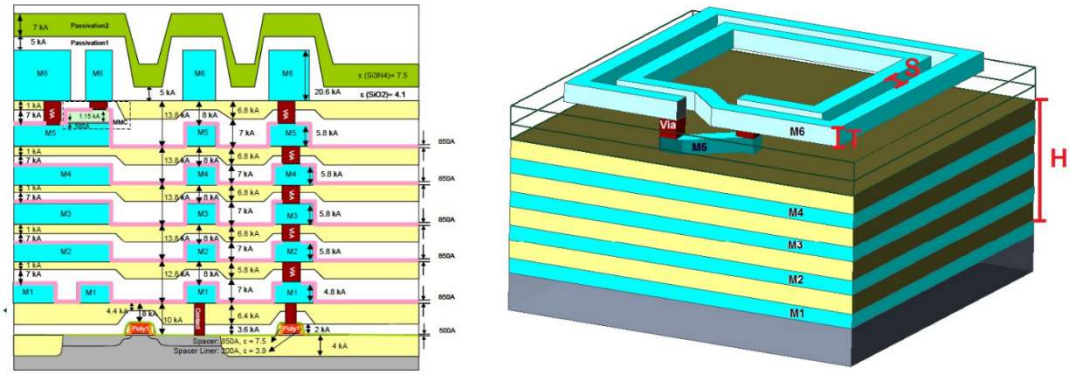


Figure 3-23. Scheme of cross-section of interconnection structure in a typical 180 um TSMC and its 3D structure [83] .

The typical cross-section view of a TSMC 180 nm process with 6 metal layers interleaved with dielectric layers is depicted in Figure 3-23. The metal M6 is the thickest metal layer of the 6 metal layers. The detailed information about the geometry of 6 metal layers and dielectric layers and their dielectric constants can be found in the TSMC user references, which cannot be shown because the information is confidential to TSMC.

Those parameters in TSMC are used to set up the HFSS simulation. The 3D HFSS setup model of the input TLT can be seen in Figure 3-24. The solid rectangular with yellow colour on the bottom of the figure represents the substrate layer, which has 700.35 μm thickness.

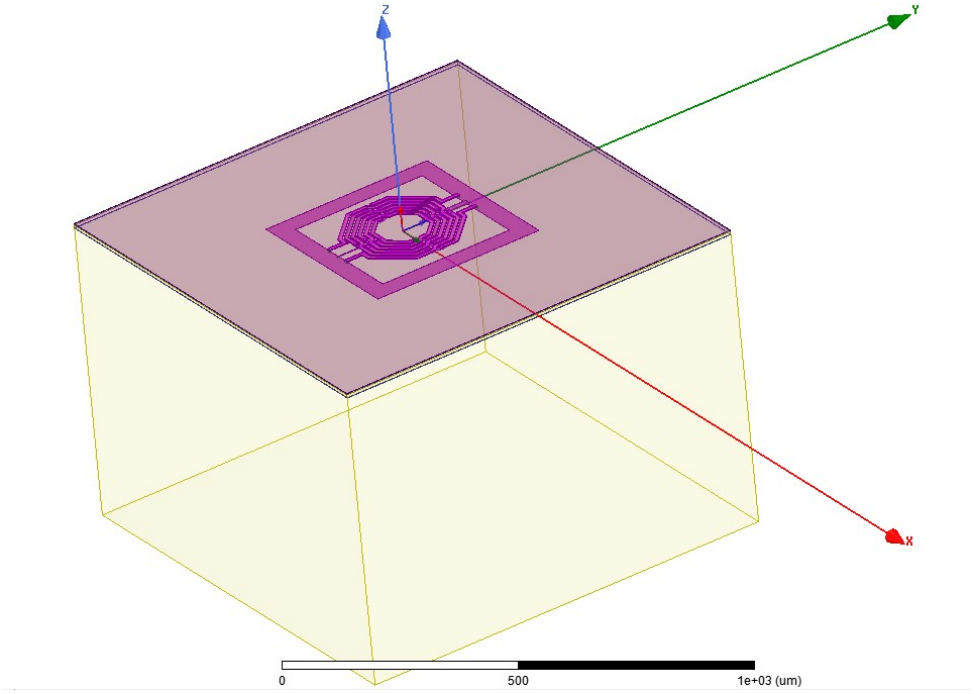


Figure 3-24. 3D HFSS setup model of the balun simulation in the TSMC substrate.

The simulated S-parameters of the HFSS simulation is put into the nport (the port in Synopsys that allows S-parameter data of n-port network, where n is an integer number) in Synopsys as shown in Figure 3-25. Here, the 6port is represented by the blue rectangular. Ports S1 and S2 in Figure 3-25 are equivalent to ports S+ and S- in Figure 3-22, respectively. Similarly, port P1 and port P2 in Figure 3-25 are equivalent to ports P+ and P- in Figure 3-22, respectively. This is a differential setting in Synopsys which uses two poles, positive and negative, of a 50 Ohm S-port. The AVSS port in Figure 3-25 is the analog ground. Port V_b and V_{DD} are equivalent to the port V_b and V_{DD} in Figure 3-22, respectively.

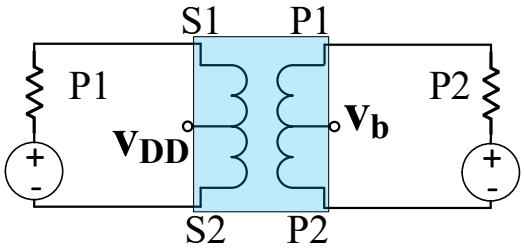


Figure 3-25. Synopsys test bed setup for extracting the L, R, Q value and coupling factor K. The test bed is used to check the self-resonant frequency as well.

The Synopsys simulation results of the inductance value and resistance of the input TLT are shown in Figure 3-26.

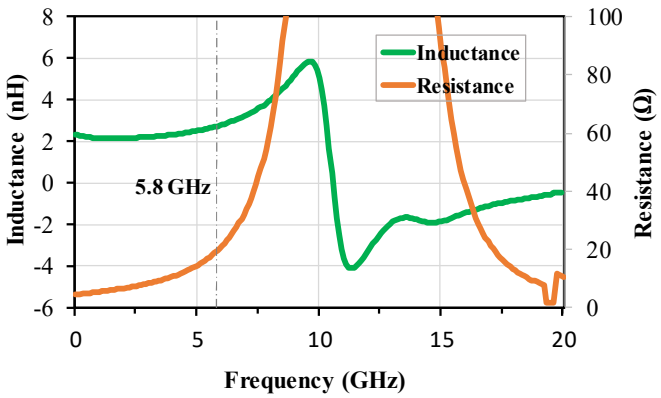


Figure 3-26. Simulated results of inductance value L (nH) and resistance value R(Ω). The self-resonace frequency is near 10 GHz where the indutance is equal to zero.

The inductance value is calculated as follows:

$$L\ (nH)\ =\ 10^9\ \frac{im(Z(1,1))}{2\pi f} \tag{3.12}$$

where L is the inductance calculated in nH, f is the operating frequency, here 5.8 GHz, $Z(1,1)$ is the impedance value of Port 1 in Figure 3-25, and $im\big(Z(1,1)\big)$is the imaginary part of the impedance value. The resistance value of the TLT is calculated as follows:

$$R\ (\Omega)\ =\ re(Z(1,1)) \tag{3.13}$$

It can be observed from Figure 3-26 that at 5.8 GHz, the inductance is 2.7 nH and R is equal to 19.5 Ω. The resistance is high because the width of the trace of the input balun is chosen to be small, only 9 µm, because the input TLT carries a very small current of the bias source V_{B1} (see Figure 3-13). Moreover, since the input TLT is a 6-ring TLT, a small width is chosen for the input TLT because it helps to save space. The inductance, which is proportional to the length of the coil, is high because the trace length of each coil is very long because the TLT has three rings on each coil.

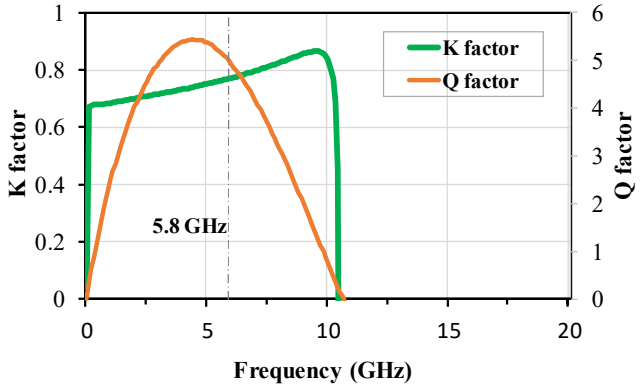


Figure 3-27. Simulated results of inductance K factor and Q factor.

The simulation results of coupling factor K and Q of the input balun is shown in Figure 3-27. The K factor and Q factor turn negative after 10 GHz which is the self-resonance frequency of the input TLT.

The Q factor is calculated as follows:

$$Q = \frac{im(Z(1,1))}{re(Z(1,1))} \tag{3.14}$$

where $re(Z(1,1)$ is the real part of the admittance value.

The Q value can be used as a measure of how much energy is lost in an inductor when it carries a sinusoidal current. Since only resistive components dissipate energy, the loss mechanisms of inductors relate to various resistances within or around the structure (due to mutual coupling) that carry current when AC current flows in the inductor. In typical CMOS technologies and for frequencies up to 5 GHz, a Q of 5 is considered moderate and a Q of 10 is considered to be relatively high [75].

The k coupling factor, based on equation (3.10), is calculated from the two-port network in Figure 3-25 as follows:

$$K = \frac{im(Z(2,1))}{\sqrt{im(Z(1,1))im(Z(2,2))}} \tag{3.15}$$

where $Z(2,2)$ is the impedance value of Port 2 shown in Figure 3-25. Z(2,1) is the impedance value between Port 1 and Port 2 shown in Figure 3-25.

The K coupling factor is 0.76 while the Q factor is approximately 5 at 5.8 GHz, as shown in Figure 3-27. It can be seen that the K factor is correlated with the k value of the interleaved type in Table 3-2. The input balun is the 6-ring balun with three rings on each coil, which has the highest coupling factor K of the interleaved type because each trace of

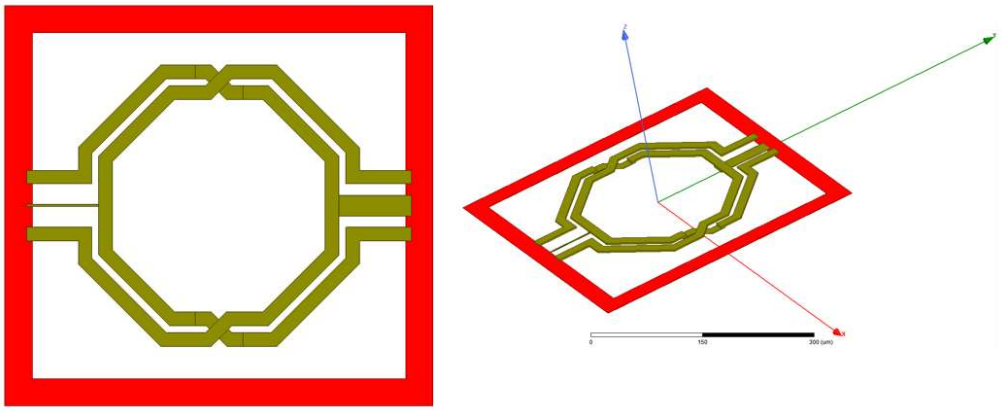


Figure 3-28. HFSS simulation model of the middle TLT.

a coil has two neighbouring traces of the other coil except the utmost outside trace and the utmost inside trace. The Q factor is low because of the high resistance R due to the long and narrow trace.

The HFSS simulation of the middle TLT can be seen in Figure 3-28.

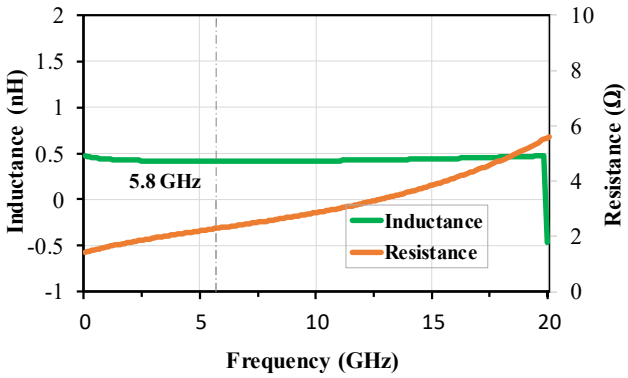


Figure 3-29. Simulated results of inductance value L (nH) and resistance value R(Ω).

The simulation results of the inductance value and resistance of the middle TLT are shown in Figure 3-29. It can be observed that at 5.8 GHz, the inductance is 0.47 nH and R is approximately 3 Ω. The inductance and resistance are low because the middle TLT has only one ring on each coil. The two-ring topology is not chosen here because it has a bigger inductance range compared to the one ring topology. The small inductance range of the one ring topology is chosen here because the parasitic capacitances, which include C_{DG} and C_{GS} of the 1st stage and 2nd stage, are big due to their big size. The width of its trace is also chosen to be 9um, which is similar to the width of the input balun for design simplicity. The DC current consumption of the 1st stage is a maximum 70 mA.

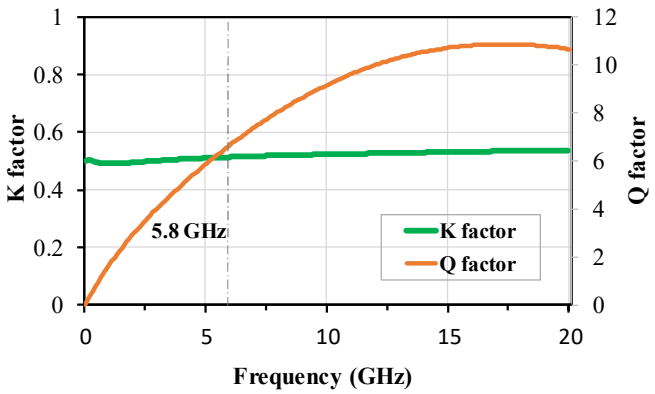


Figure 3-30. Simulated results of coupling K factor and Q factor.

It can be observed from Figure 3-30 that at 5.8 GHz, the K coupling factor is 0.513 while the Q factor is approximately 6.54. It can be seen that the K factor is in the low range of the k value of the interleaved type in Table 3-2 because each trace of a coil has only one neighbouring trace of the other coil. The Q factor is higher than that of the input TLT although they have the same 9um width of trace because of the shorter trace. The Q and K factors are heavily dependent on size (thus, the inductance) and the number of rings of the coil. Therefore, the Q and K factors are for checking if the TLT are in a reasonable design. For example, the K factors can be around the value in Table 3-2. In typical CMOS technologies and for frequencies up to 5 GHz, a Q of 5 is considered to be moderate and a Q of 10 is considered to be relatively high [75].

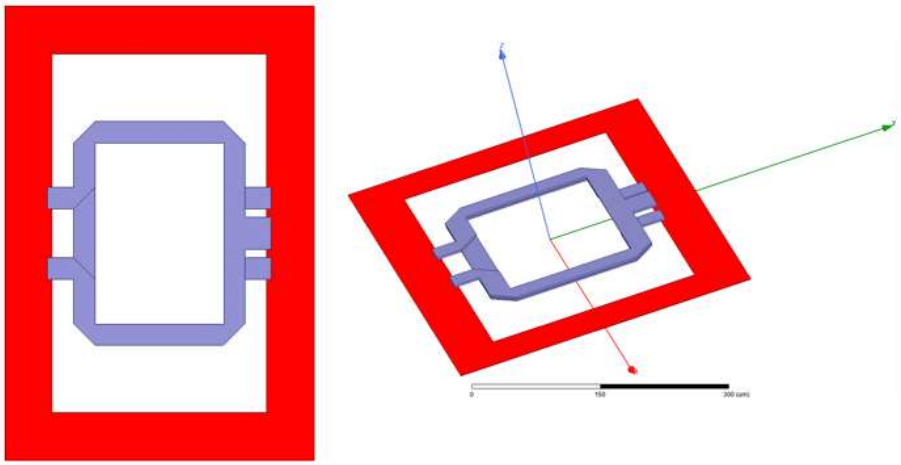


Figure 3-31. HFSS simulation model of the output TLT. The output TLT is chosen in stack type because of the higher coupling factor, thus lower loss. The rectangular shape is to keep the horizontal size of the TLT small and constant while the vertical side can be adjusted. This helps to save layout space in the horizontal size.

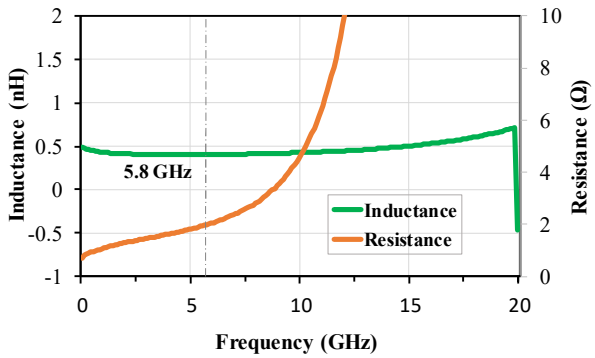


Figure 3-32. Simulated results of inductance value L (nH) and resistance value R(Ω).

The simulation results of the inductance value and resistance of the output TLT are shown in Figure 3-32. The stack type of the output TLT is chosen because it has a high

coupling factor, in the range of around 0.8 (see Table 3-2), thus having a low insertion loss. The low insertion loss at the output of the PA helps to achieve a higher P_{1dB}. The hexagonal shape must be adjusted to the radius during the optimization process, affecting both the vertical and horizontal side of the layout. The rectangular shape is chosen over the hexagonal shape because it can be chosen to have a small and constant horizontal side while the vertical side can be adjusted to a good matching. It can be observed from Figure 3-32 that at 5.8 GHz, the inductance is 0.47 nH and R is approximately 2 Ω. The inductance and resistance are low because the output balun has only one ring on each coil. While both are one-ring TLT, the resistance of the output TLT is lower than that of the middle TLT because the trace width of the middle TLT (9 µm) is much smaller. The width of its trace is chosen to be 25 µm in order to handle the big current of the power-stage, which is around 200mA at the maximum.

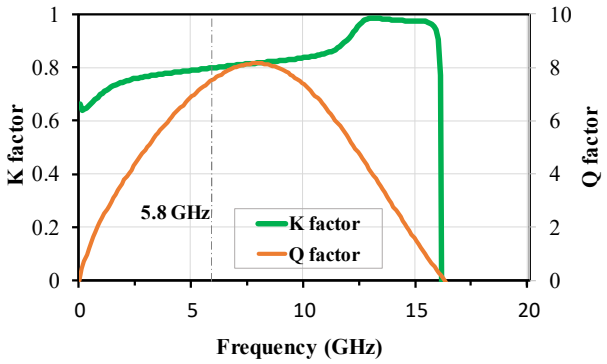


Figure 3-33. Simulated results of coupling K factor and Q factor.

The K coupling factor is 0.8 while the Q factor is approximately 7.47. It can be seen that the K factor is the highest compared to those of the input and middle TLTs. This K factor is correlated with the K value of the stacked type shown in Table 3-2. The output

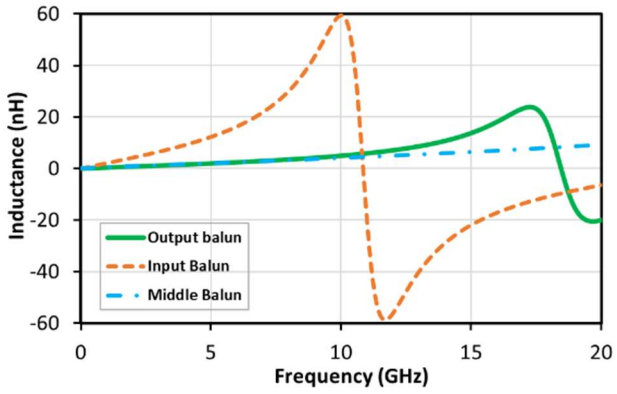


Figure 3-34. Simulated inductance of transformers. Self-resonance frequencies (cross-zero inductance line) are much higher than operating frequency 5.8 GHz.

TLT is the one-ring balun with the top metal layer (M6 layer) for the V_{DD} supply because it has the highest thickness and thus the lowest resistance.

The self-resonant frequencies of the worst-case scenario (measured with two ports of primary coil, P+ and P-, while all other ports including S+, S-, V_{DD}, and V_b, are open - meaning total reflection) in the HFSS simulation of each three TLTs are double-checked after each round of simulation to make sure that they are far away from the operating frequency 5.8 GHz, as shown in Figure 3-34. The self-resonant frequency of a TLT is a function of its electrical length because the TLT is designed based on the transmission line inductor. Therefore, the self-resonant frequency is heavily dependent on the size of the TLT. This is to make sure that the inductance values of those TLTs in the fabrication prototype are not too different from the simulated values due to manufacturing variations.

In summary, the coupling K factor, Q factor, inductance and resistance of the three TLTs are described in Table 3-3. The Q value falls between 5 to 10, which is a moderate to high value [75].

Table 3-3. Values of the three TLTs.

	K	Q	L (nH)	R (Ω)
Input Balun	0.76	5	2.7	19.5
Middle Balun	0.513	6.54	0.47	3
Output Balun	0.8	7.47	0.47	2

The three TLTs are designed in HFSS with parameter-based simulation, meaning that the size of these TLTs is changeable with a step of 10 μm in radius. The input TLT is simulated with the radius from 100 μm to 140 μm because the self-resonant frequency of the 150 um is quite near the 5.8 GHz. The 100 μm in radius is too small for the 6-ring topology. The middle TLT is simulated with a radius from 80 μm to 140 μm, where the radius range is chosen to have good impedance matching between the 1st stage and the 2nd stage at around 5.8 GHz. The output TLT is simulated with the radius from 100 μm to 200 μm. The radius below 100um of the output TLT has a very small inductance value, while the 200 um is too large in terms of space. All the simulated S-parameters are exported in Synopsys. Therefore, these results can be used to optimize the size of the CMOS transistors and MIM capacitors to achieve the design specifications.

Current Calculation of TLTs

Jmax is the maximum DC current allowed per μm or current density per μm of metal line width or per contact. The number is based on 0.1% point of measurement data at a 20% resistance increase after 10 years' continuous operation. Table 3-4 [84] shows the Jmax values of different metal layers and the rating factor to convert Jmax from one temperature to another.

Table 3-4. Jmax of Metal Line at 110° C in TSMC and its rating factor [84] .

Metal Layer	M1	M2	M3	M4	M5	M6	UTM(20kÅ)	UTM(40 kÅ)
Jmax (mA/um)	1	1	1	1	1	1.6	4	9.2
Rating factor of Jmax versus Temperature								
Temp. (C°)	70	85	100	110	125	150	175	
Rating Factor of Jmax	3.44	2.1	1.33	1	0.671	0.367	0.215	

Assuming that the PA is working at 70° C, the Jmax of the top metal layer, here is UTM(20kÅ) in Table 3-4, is equal to 4(mA/um)x3.44=13.76 mA/um. The maximum simulated currents of the 1st and 2nd stage in Synopsys in the proposed design are 71mA and 148 mA, respectively. The two currents are extracted using Synopsys Harmonic Balance (HB) simulation. Therefore, the minimum widths of the middle TLT, which are used to supply current for the 1st stage or gain-stage, and output TLT, which is used to supply current for the 2nd stage or power-stage, are 5.15 μm (=71/13.76) and 10.75 um (=148/13.76), respectively. The values are used as the minimal values of the trace widths of the middle TLT and the output TLT. In the proposed design, the trace width of the middle TLT is chosen to be 9um and that of the output TLT is 25 μm, which is much larger than the minimum values. This is to make sure that the middle and output TLTs can work at a higher temperature than 70° C.

3.2.4.3 Linearization with PMOS Adaptive Bias Circuit

The block diagram of the power-stage with the two PMOS lineariser circuits is described in Figure 3-35. Unlike the other adaptive bias linearisers in the literature, the two PMOS lineariser circuits are connected with the input and output of the 2nd stage or power-stage.

Figure 3-36 (a) shows where the PMOS lineariser is placed inside the 2nd stage of the PA. The lineariser, which is biased with V_{PMOS}, includes a PMOS transistor (M_5) and 3 resistors (R_{p1}, R_{p2}, and R_{p3}). A fraction of the output RF voltage v_{out2} of the PA is fed

through the coupling capacitor C_p to the source of M_5. The drain of M_5 is connected directly to the gate

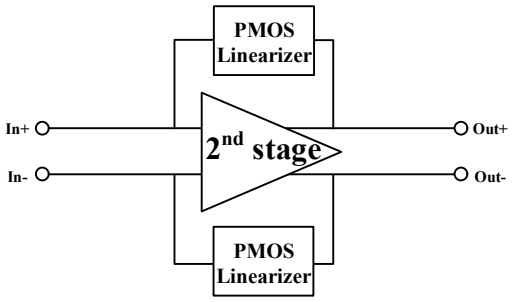


Figure 3-35. Block diagram of the 2nd stage or the power-stage with the PMOS linearizer.

of M_3. Since v_{out2} and v_{in2} are out of phase, v_{S5} (source voltage) and v_{D5} (drain voltage of

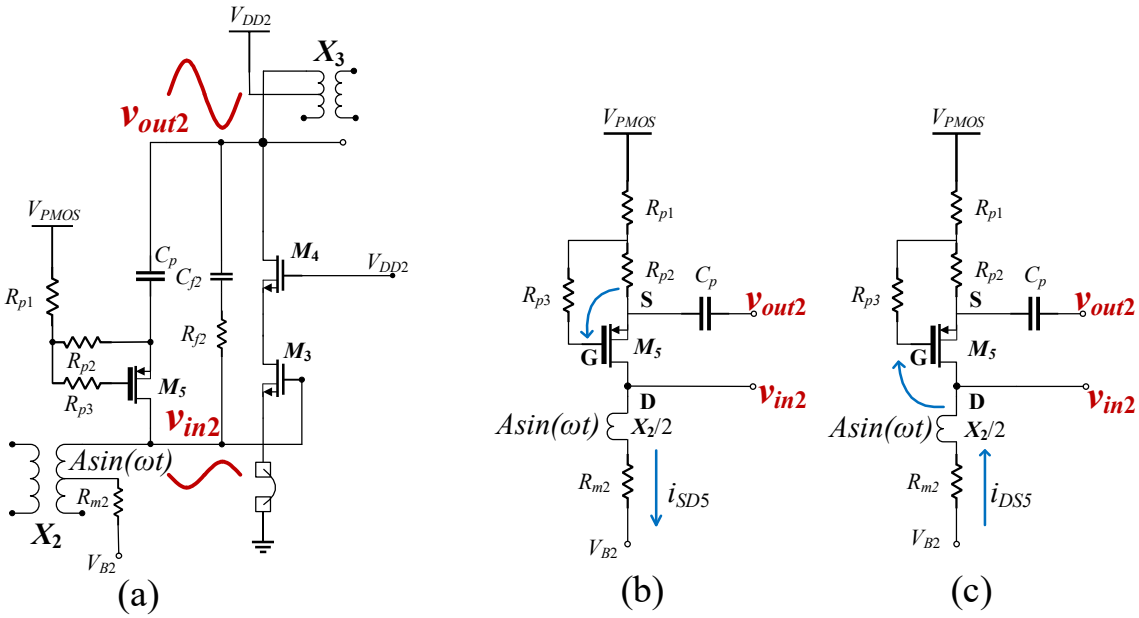


Figure 3-36. a) PMOS linearizer. (a) Schematic of the PMOS linearizer in the PA. (b) When M_5 conducts from S to D. (c) When M_5 conducts from D to S. $Asin(wt)$ is the output of the 1st stage.

M5) are out of phase. M5 is chosen as a 0.35 µm thick-gate oxide transistor to withstand the high voltage stress.

When the input power is small, the PMOS linearisers is off. As the input power level P_{in} increases, v_{SG5} and v_{DG5} of M_5 in Figure 3-36 (a) will be increased. In the half-cycle when v_{out2} is in the upper half, the PMOS linearisers circuit will let the current i_{SD5} flow from the source to the drain of M_5 when $v_{SG5} \geq V_{TH\_P}$ or:

$$v_{out2} \geq V_{TH\_P} \frac{\sqrt{(R_{p1}+R_{p2})^2 + (\frac{1}{wC_p})^2}}{R_{p2}} + V_{PMOS} \tag{3.16}$$

where V_{TH_P} is the threshold voltage of the pMOS transistor. The operation of the PMOS lineariser in this half-cycle is described in Figure 3-36 (b).

Using (3.16), the turn-on angle of the PMOS lineariser can be controlled by R_{p1}, R_{p2}, C_p, and V_{PMOS}. These parameters will be optimized for (3.16) occurring near the input 1-dB compression point IP_{1dB}. Since v_{G5} follows v_{S5} in the upper half and v_{G5} is in the lower half, $v_{SD5} > v_{SG5} > v_{SG5} - V_{TH\_P}$, M_5 always operates at saturation region when it is turned on in this cycle.

In the other half-cycle when v_{out2} is in the lower half and v_{in2} is in the upper half, the PMOS lineariser circuit will let the current i_{DS5} flow from the drain to the source of M_5 when $v_{DG5} \geq V_{TH\_P}$ or:

$$v_{D5} = v_{in2} \geq \frac{R_{p1}(v_{out2} - V_{PMOS})}{\sqrt{(R_{p1}+R_{p2})^2 + (\frac{1}{wC_p})^2}} + V_{PMOS} + V_{TH\_P} \tag{3.17}$$

Since v_{in2} is the instant output voltage of the 1st stage and is thus small, (3.17) only holds at higher P_{in} compared to (3.16). The operation is described in Figure 3-36 (c). However, (3.17) rarely occurs in a practical operation because it occurs at very high input power.

The currents i_{SD5} and i_{DS5} will change the average value or the DC value of v_{in2} (bias voltage of M_3) through R_{m2} and X_2.

The DC value of v_{in2} can be expressed [85] as follows

$$V_{in2} = \frac{1}{2\pi}\int_0^{2\pi} v_{in2}\, d(wt) \tag{3.18}$$

where

$$v_{in2} = \begin{cases} V_{B2} + Asin(wt) + i_{SD5}(R_{m2} + \dfrac{Z_{X2}}{2}) \; when\ (1) \\ V_{B2} + Asin(wt) - i_{DS5}(R_{m2} + \dfrac{Z_{X2}}{2}) \; when\ (2) \\ V_{B2} + Asin(wt) \quad otherwise\ \ (M_5\ turns\ off) \end{cases} \tag{3.19}$$

where Z_{X2} is impedance of X_2.

In the case of the conventional PA without the PMOS lineariser, $v_{in2} = V_{B2} + Asin(wt)$. Since the average value of $Asin(wt)$ in one cycle is equal to zero, $V_{in2} = V_{B2}$, meaning no adaptive bias, as seen in Figure 3-37(a).

Figure 3-37(a) shows that V_{in2} adaptively follows P_{in} with different values of V_{PMOS}. V_{in2} is raised by i_{SD5} (3.16), from V_{B2} (0.58V) to higher values around the IP_{1dB} of 0 dBm. At higher input power, V_{in2} is decreased by i_{DS5} (3.17). Furthermore, when V_{PMOS} increases,

i_{SD5} increases as well, leading to the increment of the bias voltage V_{in2}. Therefore, the V_{PMOS} can be controlled to tune the linearity of the fabricated prototype in order to mitigate the discrepency between simulation and measurement.

Figure 3-37(b) compares the simulated power curves of the conventional PA to the proposed PA with three different widths of M_5. When the width of M_5 increases, the current drawn from V_{PMOS} increases as well, leading to an increment of voltage drop across R_{p1} and R_{p2}. Therefore, the bias voltage V_{in} reduces, leading to a reduction of gain expansion. It also shows that the OP_{1dB} of the proposed PA increases to 18.7 dBm from 16.1 dBm of the conventional PA, meaning a 2.6 dB improvement. Furthermore, unlike the cold-FET linearisers in [15, 16], which require 1 to 2 dB insertion loss to linearize PAs, the proposed PMOS lineariser does not introduce any insertion loss when compared to the conventional PA.

Therefore, by appropriate selection of VPMOS, width of M_5, together with other parameters including R_{p1}, R_{p2}, R_{p3}, R_{m2}, and C_p, the desired adaptive bias characteristics can be achieved.

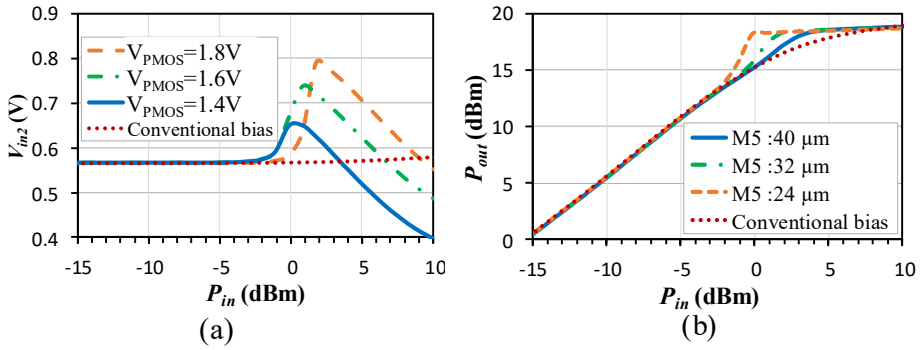


Figure 3-37. Simulated two parameters versus P_{in}. (a) V_{in2} with different V_{PMOS}. (b) P_{out} with different widths of M_5.

3.2.4.4 Small Signal and Large Signal Stability

Stability is one of the most important considerations in designing a power amplifier. The small signal stability is the Rollett stability factor, k, which is based on S-parameter data. The stability k-factor needs to be greater than unity across frequencies, here 0 GHz to 10 GHz, then the amplifier with input and output matching is in a stable condition. The stability k-factor is mostly useful for the single-stage amplifier. However, it can still be useful for the two-stage amplifier since it can be utilized to check small signal stability. The stability k-factor can be calculated directly from the S-parameters using equation (2.2).

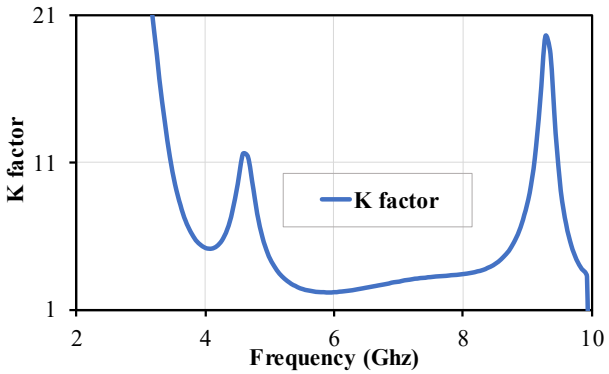


Figure 3-38. A sample of the simulated k factor versus the frequency of the whole PA in the schematic simulation. The k factor can also be calculated directly from the simulated S-parameters. The k factor must be larger than 1 in all frequencies.

The small signal stability k factor is only valid with a small disturbance (meaning the PA is injected with small input power). For larger input power or a large signal stability check, a transient simulation approach to excite the oscillator circuit is proposed to check for potential oscillations of the entire two-stage amplifier. An oscillator will oscillate easily if it is injected with disturbances including noise or impulses. The transient simulation setup will introduce a wide range of disturbances, including input disturbances and voltage supply disturbances, into the PA circuit to see if any oscillations occur. The transient period is set to 100ns due to limitations in simulation time. Figure 3-39 and Figure 3-40 show the test circuit for potential oscillations. In Figure 3-39, an input transient signal with amplitude of the input P_{1dB} in turned on-off. The frequencies of the transient signal are from 1 GHz to more than the third harmonic frequency of 5.8 GHz. The output transient response should

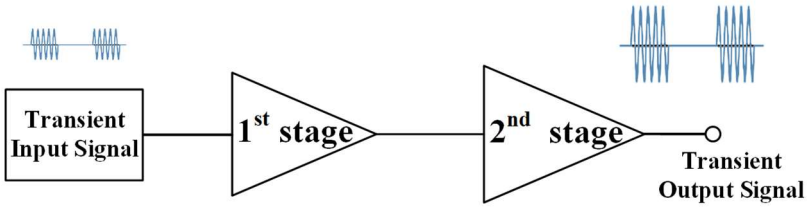


Figure 3-39. Test circuit in simulation for stability, on-off input signal.

be zero after each period. If the output signal keeps ringing, then the amplifier will not be stable and oscillate. Then, the root cause must be found, not only in the feedback parts of the PA including the bond wires and RC feedback, but also in the bias and matching circuit as well.

In Figure 3-40, the VDDs of the 1st and 2nd stage amplifiers are turned on-off while the input signal is a continuous 5.8 GHz signal to test the stability of the PA. If the output signal keeps ringing, then the amplifier will not be stable and oscillate. Then, the root cause must

be found, not only in the feedback parts of the PA including the bond wires and RC feedback, but also in the bias and matching circuit as well.

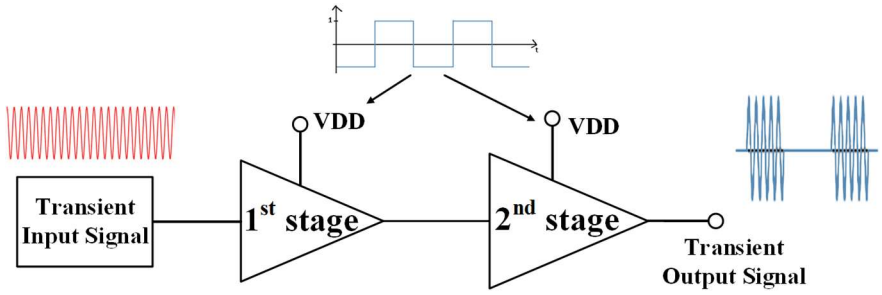


Figure 3-40. Test circuit in simulation for stability, on-off supply voltages.

3.2.5 PA Layout Design

3.2.5.1 Layout

The layout of the whole PA is implemented using the layout optimization method in [86], which can minimize lossy resistance of interconnection by utilizing the two large metal layers for the transistors' source and all six metal layers for their drain. The 3D layout can be seen in Figure 3-41. The gates of the transistors are connected from metal layer 1 to metal layer 6 to reduce the resistance of the interconnection. Layer 6 is then used to connect the gates and drains to different parts of the circuit to reduce the lossy resistance of the interconnection because it is the thickest metal layer. The simulation predicts that the total gate resistance is reduced by about 40% with double-side connections [86]. The drains of the transistors are connected using a similar method and run on top of the transistors. This method reduces the overlap between the gate and drain of the transistors and thus, reduces C_{GD} which can degrade gain performance significantly at a high frequency due to the negative feedback (drain voltage and gate voltage are opposite in phase in a common source amplifier). Because both the gate and drain are connected through thick metal layers, the interconnect resistance is also minimized. The source and buck of the transistors are connected through the wide metal track of layer 1 and 2. This layout can easily be duplicated to construct a large transistor for power amplification with minimized interconnected parasitics.

The schematic and the corresponding layout of the 1st stage is represented in Figure 3-42 and Figure 3-43.

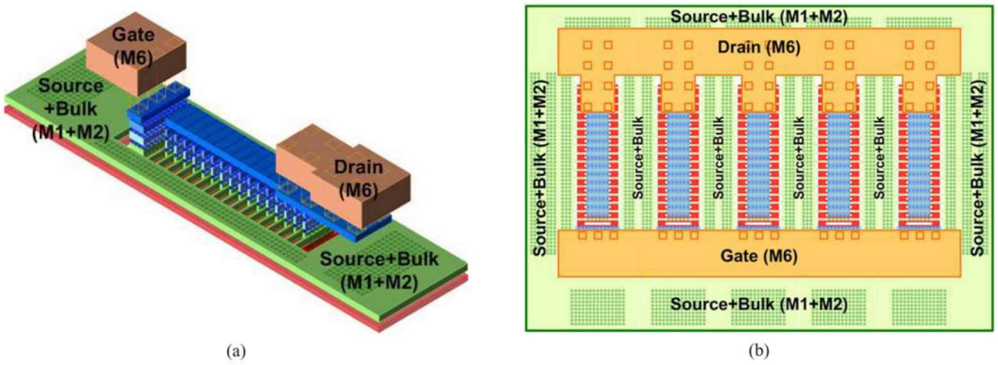


Figure 3-41. The 3D layout in [86]. (a) 3D layout of a single unit. (b) 2D layout of 5 units. The gate and drain of transistors are connected from metal layer 1 to metal layer 6 to reduce parasitic resistance.

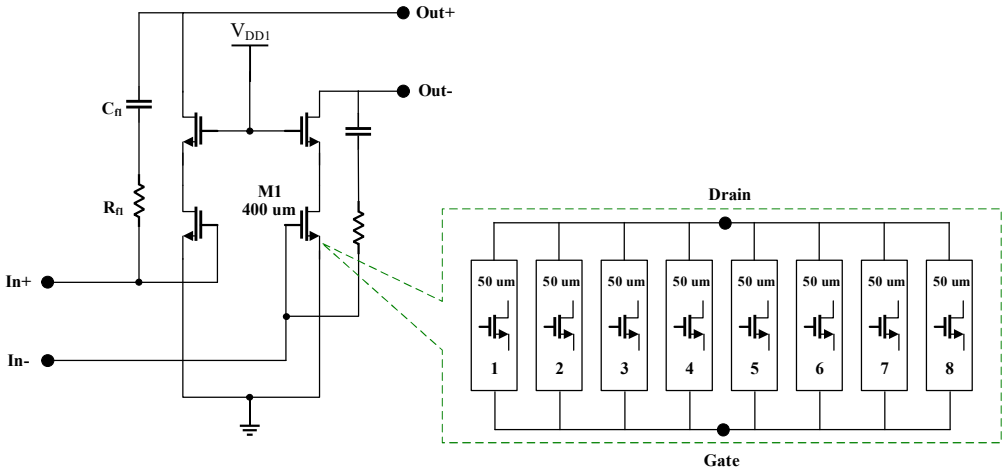


Figure 3-42. Schematic of the 1st stage. The M1 transistor is divided into 8 parallel transistors.

Figure 3-42 shows the schematic of the 1st stage. The total width of each transistor M1 is 400 µm, including 8 transistors in parallel to reduce parasitics. Each transistor contains 25 fingers which are 0.18 µm in length and 2 µm in width. Figure 3-43(a) shows the layout drawing of a single transistor unit using the layout optimization method in Figure 3-41. Figure 3-43(b) describes the total layout of the 1st stage using the layout optimization method in Figure 3-41. The top metal layer 6 trace is used to connect signal in and signal out to the 1st stage since it has the lowest resistance.

Similarly, the schematic and layout of the 2nd stage or the power stage are shown in Figure 3-44 and Figure 3-45. Figure 3-44 shows the schematic of the 2nd stage. The total width of each cascode transistor M4 is 828 µm, including 9 transistors in parallel. The total width of each transistor M3 is 1104 µm, including 12 transistors in parallel. Each transistor contains 46 fingers, which are 0.18 µm in length and 2 µm in width. Figure 3-45(a) describes the layout of a single transistor unit using the layout optimization method in Figure 3-41. Figure 3-45(b) describes the total layout of the 2nd stage using the layout

optimization method in Figure 3-41. The top metal layer 6 trace is used to connect the signal in and signal out to the 2nd stage since it has the lowest resistance.

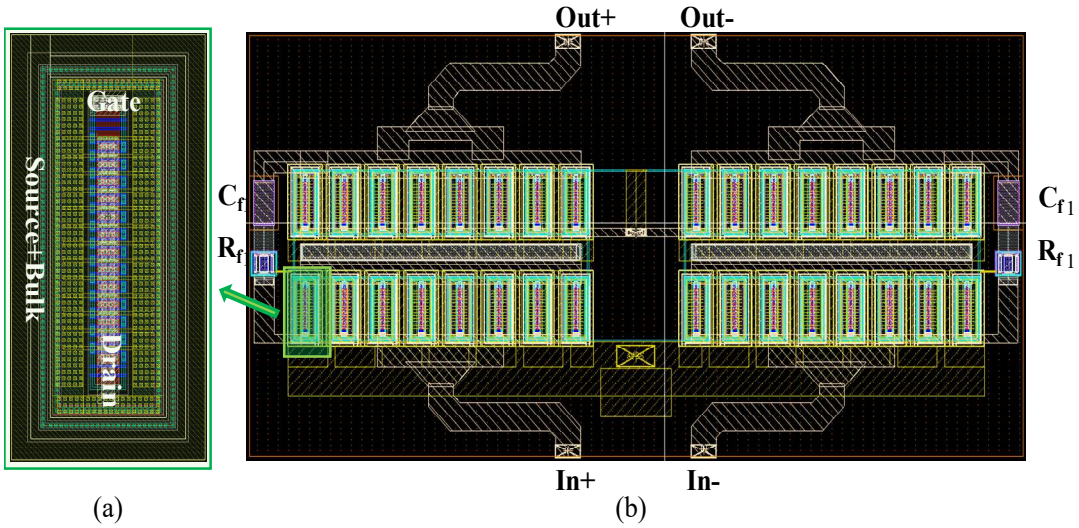


Figure 3-43. (a) Layout of a transistor containing 25 fingers of 2 µm width for each finger. (b) Layout of the 1st stage. The feedback capacitor and resistor are C_{f1}=0.4pF and R_{f1}=604 Ω, respectively.

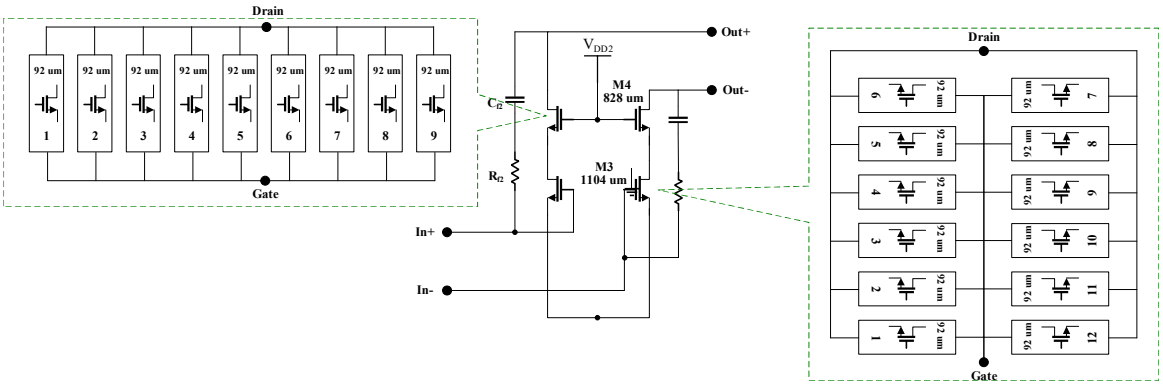


Figure 3-44. Schematic of the 2nd stage. The layouts of M3 are folded to save space.

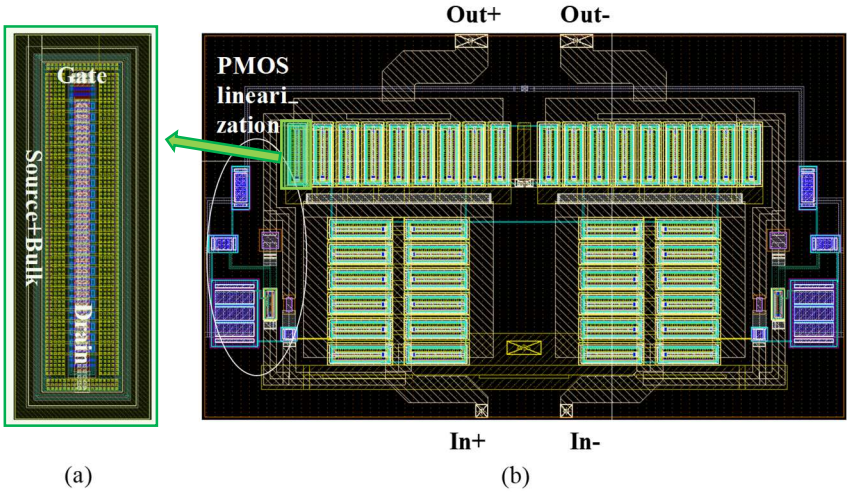


Figure 3-45. (a) Layout of a transistor containing 46 fingers of 2 µm width for each finger. (b) Layout of the 2nd stage with PMOS linearization.

All the transistors in the 1st stage and 2nd stage are characterised using the post-layout simulation of individual transistors to work out the parasitic capacitors and resistors. Then, the transistor models with all the parasitic resistors and capacitors are put in the Synopsys simulation to increase the accuracy of the simulation compared to using schematic transistors from Synopsys PDK.

Figure 3-46 shows the layout of the two-stage PA. Three TLTs are placed in a straight line with the 1st stage and the 2nd stage.

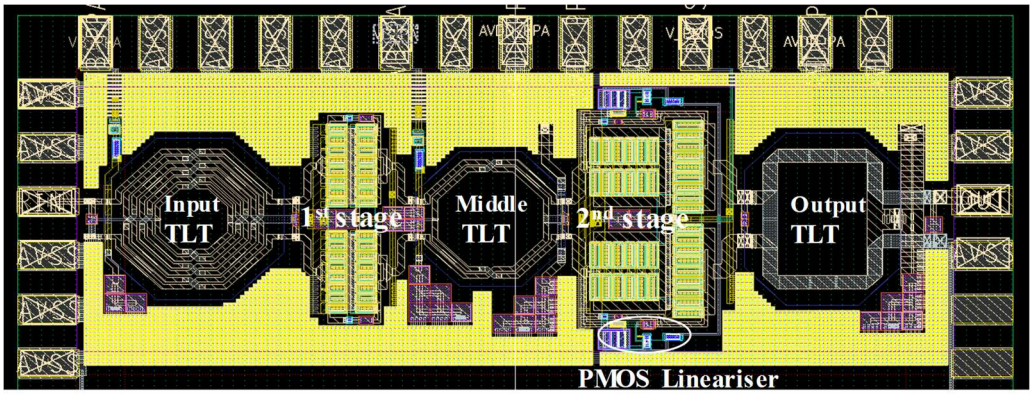


Figure 3-46. Die micro-photo of the proposed PA. The chip size is 1.441 x 0.543 mm2 including the fillers in the yellow colour.

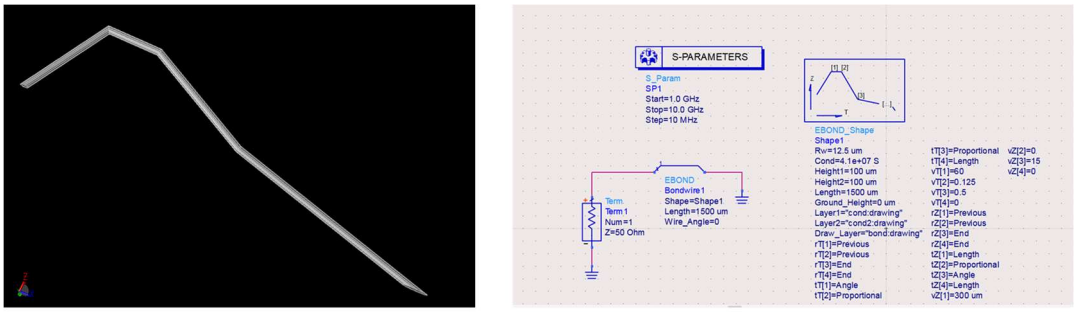
3.2.5.2 Bondwire Equivalent Models

Since the parasitic sources from the bondwire significantly affect the power amplifier performance, the entire power amplifier test circuit should include bondwire parasitic models during the Synopsys simulation.

The normal bondwires connect the bond pad in the chip, or chip pad, to the pin lead in the package, or packaging pad, as shown in Figure 3-47.

Figure 3-47. Bondwire in a chip [87].

The 3D model of a normal bondwire in ADS and the ADS simulation setup to find the equivalent circuit is shown in Figure 3-48(a) and (b), respectively. The material of the bondwire is gold. Its length is 1500 µm and its diameter is 25 µm.



(a) (b)

Figure 3-48. (a) 3D model of a bondwire in ADS, (b) ADS simulation setup.

The normal bondwires can be modelled with passive components including a resistor connected with an inductor. The package pad and the chip pad are modelled as lumped capacitors since both the pads form metal-insulator-metal (MIM) capacitors. The resistance and inductance values of the normal bondwire can be calculated using S-parameters from the ADS simulation in Figure 3-48. Then, from the S-parameters, the resistance and inductance can be extracted using equations (3.12) and (3.13), respectively. The values of the C_{pakage_pad} and C_{chip_pad}, which are MIM capacitors, are calculated based on information supplied in TSMC design kits and chip packaging. The formula for the capacitance calculation of an MIM capacitor can be found in Chapter 4.

The equivalent circuit model of a normal bondwire is shown in Figure 3-49(a) and its simulation setup in Synopsys is shown in Figure 3-49.

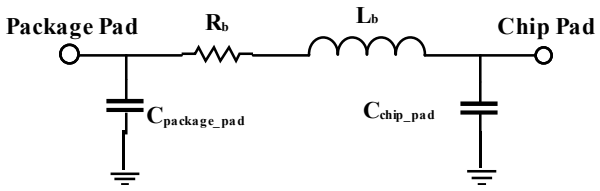


Figure 3-49. Equivalent circuit model of a bondwire. The values used in this design are: R_b=0.056 Ω, L_b=1.37 nH, $C_{package\_pad}$=0.416 pF, and C_{chip_pad}=0.12pF.

The normal bondwire diagram of the proposed PA is shown in Figure 3-50. The empty space below the PA but inside the chip area is left for other chips from other projects.

The ground bondwires, connected from the chip pad to the ground thermal pad of the chip, not to the package pad, have half values of resistance and inductance of the normal bondwires stated above and do not have the capacitor C_{pakage_pad}. The reason for this is that the length of a ground bondwire is approximately half that of the bondwire. The equivalent model of a ground bondwire is shown in Figure 3-51.

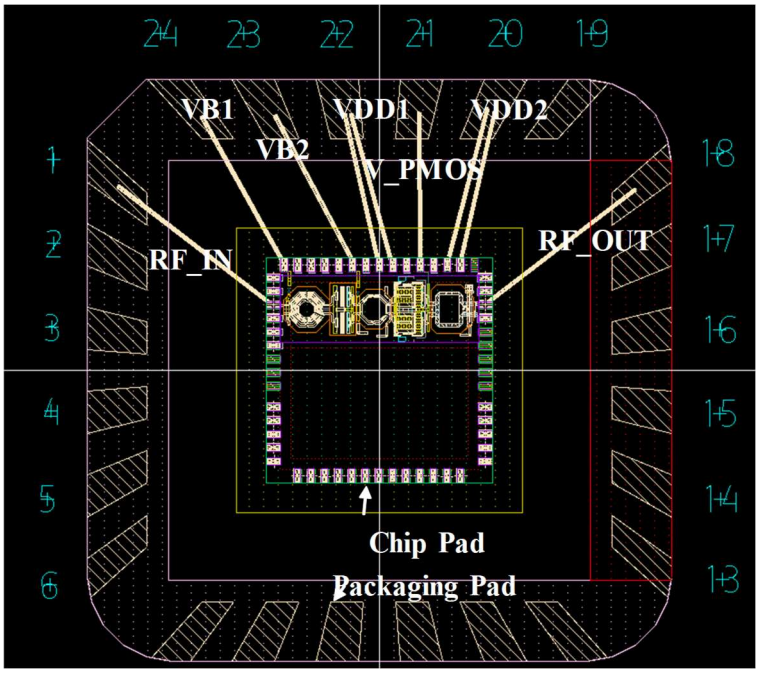


Figure 3-50. The normal bondwire diagram of the proposed PA. The normal bondwires connect the bond pad in the chip, or chip pad, to the pin lead in the package, or the packaging pad.

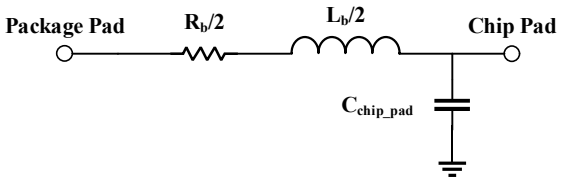


Figure 3-51. Equivalent circuit model of a ground bondwire.

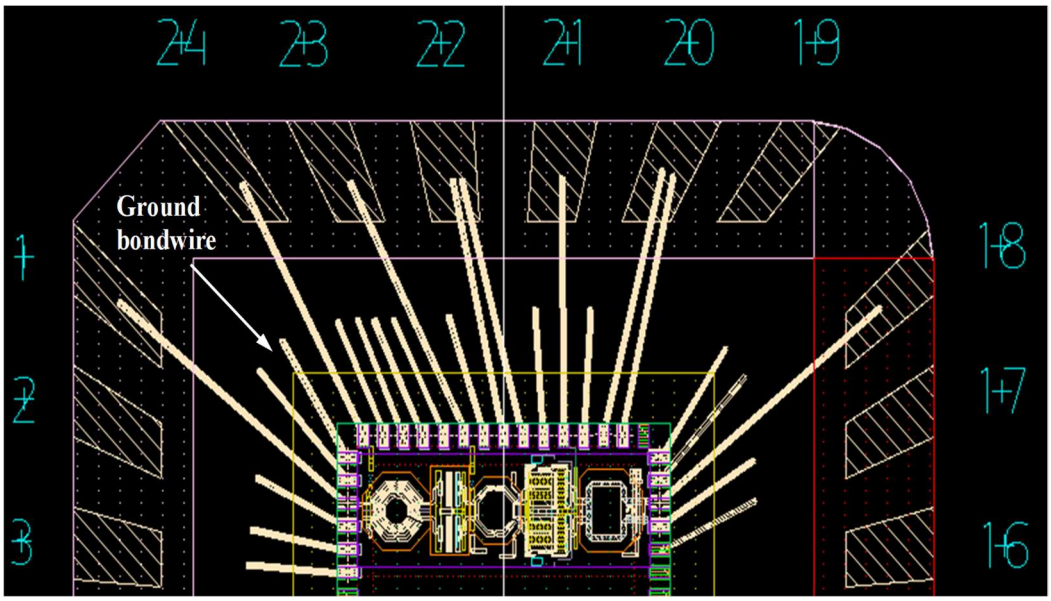


Figure 3-52. The ground bondwire diagram of the proposed PA. The ground bondwires (shorter ones) are connected from the chip pad to the ground ring of the chip, not to the package pad

The ground bondwire diagram of the proposed PA is shown in Figure 3-50 There are 27 ground bondwires in the chip, therefore the PA circuit is also designed and simulated with 27 ground bondwires. All these values were used in the schematic and used during the design/simulation process. The number of ground bondwires does not greatly affect the S-parameters of the PA, but it strongly affects the stability of the PA through the k stability factor. The effect is due to the substantial transient voltages produced across the bondwires connected to the ground [75]. The larger the number of ground bondwires, the less positive feedback at the source of transistors, and thus, the better the k stability factor and vice versa.

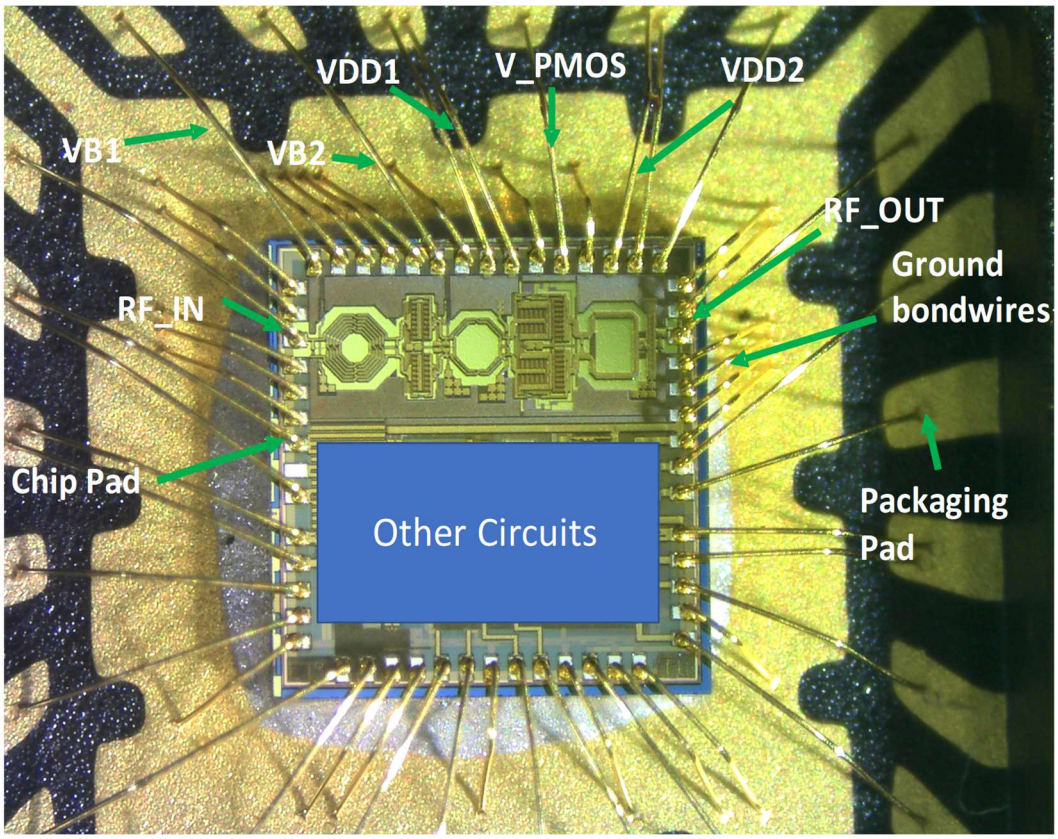


Figure 3-53. The fabrication photograph of the proposed PA.

3.3 Implementation and Experiment Results

3.3.1 Printed Circuit Board (PCB) Design

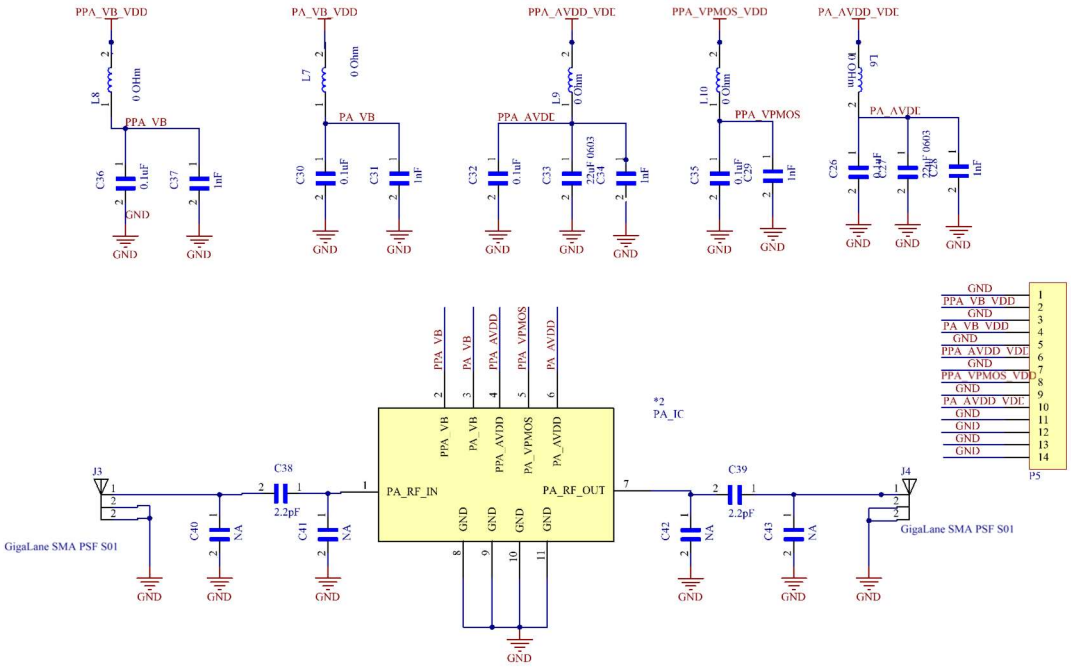


Figure 3-54. PCB schematic for the proposed PA. The capacitors 0.1 uF, 22 uF, and 1 nF are used to filter noise from the DC power supplies. Two high RF quality GigaLane SMAs are connected to the RF input and RF output of the PA chip through coupling 2.2 pF caps. Here, PPA coresponds to 1st stage and PA coresponds to the 2nd stage.

The RF PCB for the PA chip is developed and built to measure the power amplifier performance. The schematic shown in Figure 3-54 is designed for the proposed PCB. The PCB layout includes a two-port single-ended input and output. The PCB layout size which was fabricated is 62.5mm×61.7mm, which is shown in Figure 3-55.

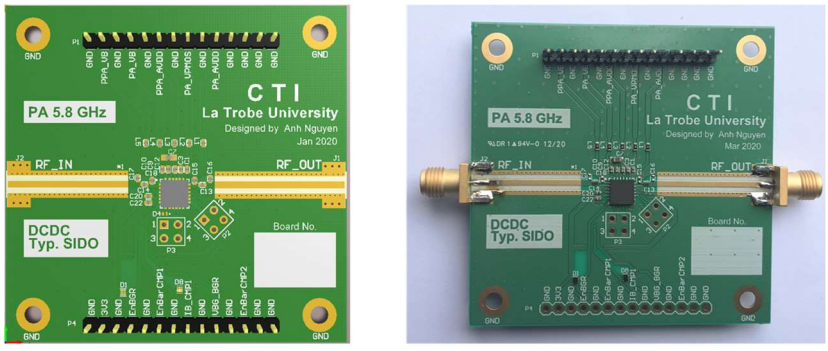


Figure 3-55. (a) Altium 3D view of PCB layout for the proposed PA.(b) The fabricated prototype has soldered GigaLane SMA connectors and other soldered components. Here, PPA coresponds to 1st stage and PA coresponds to the 2nd stage.

The test board picture is fabricated with the high frequency laminate Roger RO4003C. Figure 3-55 shows the packaged power amplifier, SMA connectors, bypass caps for power

voltage supplies and bias voltage supplies. The matching circuits at the signal lines RF_IN and RF_OUT is for matching the 50 Ohm CPW line to the small pin of the packaged power amplifier.

3.3.2 Power and S-parameter Measurement Test Setup

After the PCB prototype is fabricated and the packaged power amplifier with auxiliary circuits are soldered, the measurement can be taken. The S-parameter and P_{1dB} compression characteristics of the power amplifier are measured using the network analyser and spectrum analyser in the setup shown in Figure 3-56 and Figure 3-57. A 20dB attenuator is used because the input capability of the equipment, such as the network analyser and spectrum analyser, are only 20dBm. Both the 1dB gain compression and 1dB output power compression of the amplifier at the operating frequency can be found from this measurement. Network analyser calibration is achieved with a typical SOLT standard kit at a certain power level before performing the measurement.

3.3.3 Measurement Results

The proposed PA is fabricated in TSMC 20K2f 0.18 μm CMOS technology, and occupies an area, including pads, of 1.07 mm^2. The microphotograph of the PA is shown in Figure 3-58.

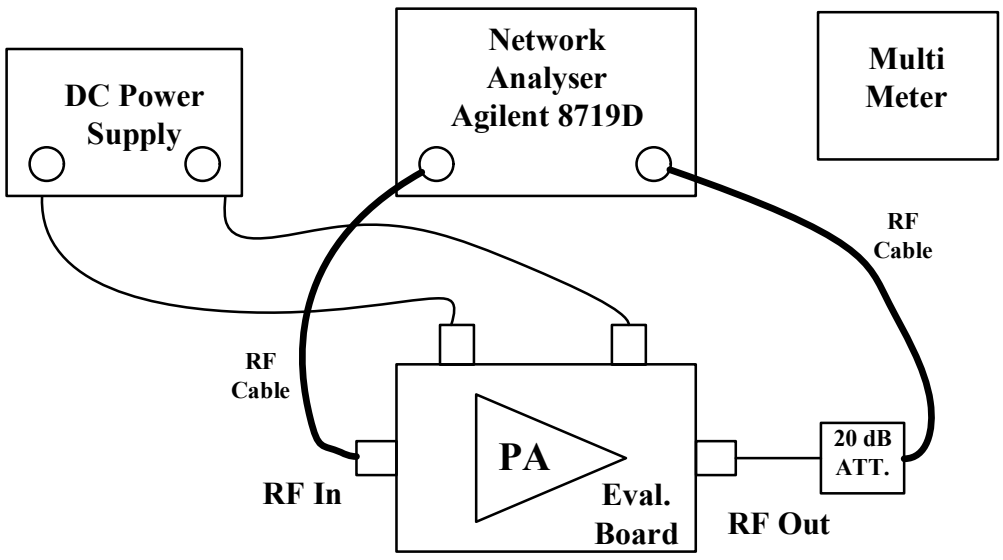


Figure 3-56. Test setup for S-parameter measurement.

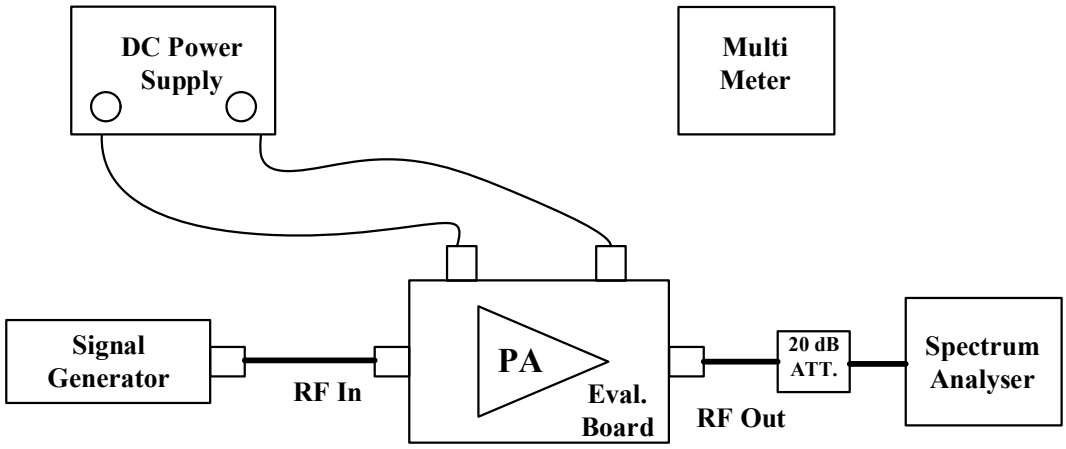


Figure 3-57. Test setup for power_out/power_in curve measurement. The P_{1dB} can be read from this curve.

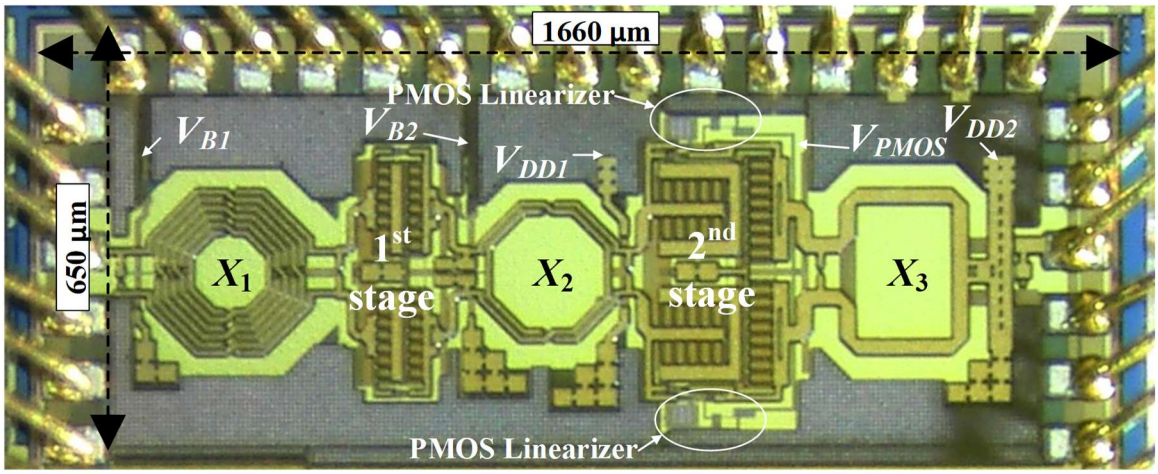


Figure 3-58. Microphotograph of the fabricated PA. The size is 1.660 x 0.650 mm^2.

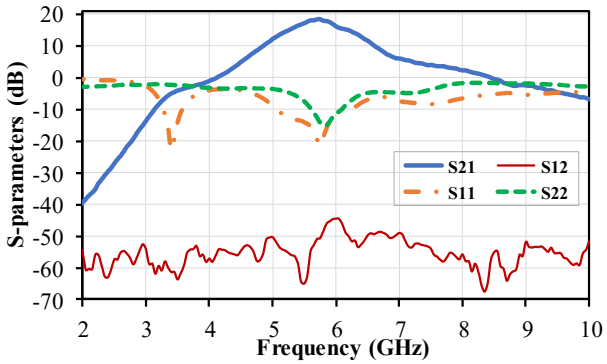


Figure 3-59. Measured S-parameters of the whole PA.

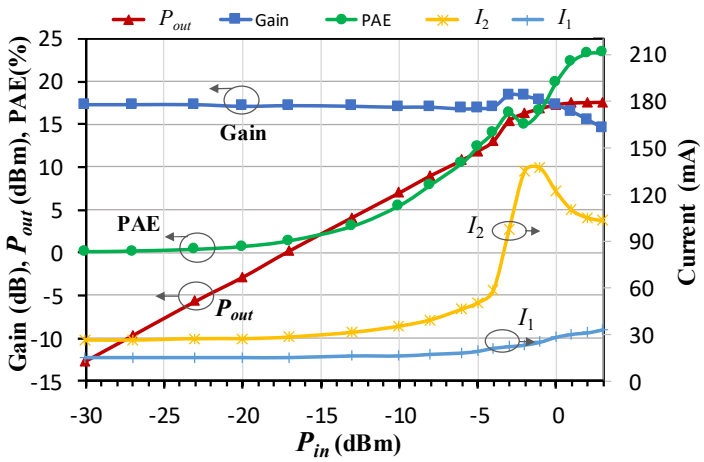


Figure 3-60. Measured PAE, gain and power curve of the whole PA.

The measurement results in Figure 3-59 show that the small signal gain of the proposed PA is 18 dB while the reverse isolation is 48.5 dB at 5.8 GHz. The high isolation can prevent the local oscillator (LO)'s frequency from pulling due to a sudden output load change.

The input and output return loss are larger than 10 dB at 5.8 GHz. Figure 3-60 shows that the measured OP_{1dB} is 17.5 dBm at IP_{1dB} of 0.5 dBm and the corresponding $PAE@P_{1dB}$ is 22.5 %. The P_{SAT} is also 17.5 dBm. The measured consumption current I_1 of the 1st stage is almost unchanged for the input power sweep. However, the 2nd stage current I_2 increases dramatically at high input power because V_{B2} is increased by the PMOS lineariser. The gain expansion can be observed at the input power range from -4 dBm to 1 dBm due to the impact of the PMOS lineariser. The bumps of *PAE* and the DC current I_2 of the 2nd stage at the input power around -3 dBm occur for the same reason. As a result of the gain expansion, the OP_{1dB} is equal to the P_{SAT}.

Table 3-5 summarizes the overall performance of the proposed PA in comparison with previous works. In terms of its overall performance, the proposed PA achieves a high figure of merit (*FOM*) of 64.38, which considers saturation power, gain, efficiency, and operating frequency all together [86, 88]. In addition, although operated with the lowest supply voltage, the PA dissipates the smallest quiescent current. A low quiescent current saves the PA's power consumption in low/normal power transmission conditions which occurs the majority of the time. It also achieves a very high isolation. The work in [39] achieves higher *FOM* at the expense of very high quiescent current, high voltage supply, and large chip size.

Table 3-5. Performance comparison.

PERFORMANCE COMPARISON

References	[39]	[14]	[89]	[15]	**T.W.**
CMOS process (μm)	0.18	0.18	0.18	0.18	**0.18**
Topology	Diff.	Single-ended	Single-ended	Single-ended	**Diff.**
Linearity techniques	NMOS diode	Doherty& Adaptive bias	Doherty	Built-in NMOS lineariser	**PMOS adaptive bias**
Frequency (GHz)	5.25	2.4	2.4	2.4	**5.8**
Supply Voltage (V)	2.4	3	3.3	2.4	**1.8**
Gain (dB)	20	10.6	12	20	**18**
Isolation (dB)	NA	23	NA	30	**48.5**
OP_{1dB} *(dBm)*	16.5	21	21	20.6	**17.5**
PAE @P_{1dB} *(%)*	20	33	14	24.6	**22.5**
P_{SAT}	20.9	22.3	21	22	**17.5**
PAE @P_{SAT} *(%)*	20	21	14	30	**23**
Quiescent current (mA)	156	NA	NA	95	**44**
Chip Size (mm^2)	1.32	0.54	2.76	1*	**1.07**
FOM	68.31	53.72	52.06	64.37	**64.38**

All chip sizes include pads.

* did not mentioned the pads

FOM= P_{SAT} *(dBm) + Gain (dB) +10log(PAE@*P_{SAT} *(%))+20log(freq (GHz))*

3.4 Summary

A cascode differential PA with a novel built-in PMOS lineariser is proposed using TSMC 0.18 μm CMOS process technology. The PMOS lineariser is proven to work as an adaptive bias circuit using Kirchhoff equations. The lineariser senses the strength of the input and output RF signal of the PA stage and converts the signals into a proper DC bias of the power amplifier. This technique mitigates the existing issues of the recent adaptive bias techniques including complex and big schematic and high DC current consumption.

A cascode differential PA at 5.8 GHz has been designed with a new built-in PMOS lineariser using TSMC 0.18 μm CMOS process technology. The fabricated chip demonstrated OP_{1dB} of 17.5 dBm with a PAE of 22.5%. The quiescent current is 44 mA and the reverse isolation is 48.5 dB. The proposed PA achieves a high *FOM* of 64.4 with a small chip size of 1.07 mm^2.

The PA achieves competitive performance with the lowest DC quiescent current, small chip size and moderate P_{1dB} at the highest frequency and the lowest supply voltage compared to the state-of-the-art PAs in the literature. Furthermore, the proposed PA has noise immunity due to its differential structure, which is not available in the single-ended structure. With this improvement in P_{1dB}, the PA meets the demand of high linearity in modern wireless communications with higher peak-to-average power ratio (PAPR) standards. The high PAPR allows a large number of independently modulated subcarriers, thus leading to a high data rate transmission.

However, the PA alone cannot achieve the four goals of miniaturization, high data rate, longer battery lifetime, and lower cost for RF components. To do this, the biggest part of the RF components, the antennas, are in consideration because they are the direct input/output load of RF transceivers. The efficient performance of the PAs and the harmonic components emitted by the PAs can be improved by optimizing the direct output load. Moreover, the noise and interference immunity of the LNA can be increased further by improving their direct input load which is the antenna.

Chapter 4 discusses harmonic suppression antennas and how they help to attain the goal of miniaturization, longer battery lifetime, and lower cost. With their small size, the proposed antennas can be integrated into portable wideband devices.

4 Harmonic Suppression Antennas

The motivations of this thesis focus on improving the important features of RF components namely miniaturization, high data rate, longer battery lifetime, and lower cost for RF components. Chapter 3 discussed power amplifiers (PAs) with the PMOS linearity technique to increase P_{1dB}, which can achieve a high PAPR, and thus the high data rate goal. A novel adaptive bias circuit is proposed utilizing both the output and input signals of a PA. This technique mitigates the existing issues of the recent adaptive bias techniques, namely their complex and large design and high DC current consumption. However, the efficient performance of the PA and the noise immunity of the LNA can be increased further by improving their direct input/output loads, which are antennas. This chapter discusses harmonic suppression antennas and how they help to attain the goal of miniaturization, longer battery lifetime, and lower cost. With their small size, the proposed antennas can be integrated into portable wideband devices.

Antennas are connected to the PA and the low noise amplifier (LNA) through a switch and a filter. Therefore, the performance of the antenna affects the overall performance of the RF transceiver in general and the performance of PA and LNA specifically. Specifically, the higher-order harmonic components should be suppressed to improve the power added efficiency (PAE) of the PA in the transmitter [18, 19]. As a result, the power consumption performance of RF transceivers is enhanced, leading to longer battery lifetime. The suppression also helps reduce those components emitting to other communication devices. On the receiver side, harmonic suppression is required to cancel out-of-band noise and interference [20-23] to improve the data rate. Therefore, a filter between the antenna and the RF transceiver is needed to achieve better noise, thus improving the data rate of communication systems.

Filters are generally used in series with the antenna to suppress unwanted high-order harmonics or interference. However, the filter insertion approach fails to achieve miniaturization and often increases insertion loss and thus, leads to an increase in total implementation cost and performance degradation of the whole system. Hence, an antenna with inherent out-of-band rejection capable of rejecting unwanted radiations and suppressing higher-order harmonics is a more cost effective and area efficient alternate approach. As a result, the harmonic suppression antenna meets the requirement for further miniaturization by reducing the size of the RF circuit system. Chapter 2 provides details of the literature review in relation to harmonic suppression techniques, including DGS,

stepped slot, and thin microstrip line and MIM cap. The existing issues facing these techniques are increased size, bandwidth reduction, and weak suppression in the rejection bandwidth. In this chapter, some new harmonic suppression techniques are proposed to mitigate these issues without affecting the gain and radiation pattern.

The DGS technique is combined with the stepped slot technique to provide a harmonic suppression capability for the two narrow slot antennas. The proposed combined technique in these two narrow antennas mitigates the problem of the increase in size in the previous DGS works. Moreover, the combined technique solves the issue of not having enough suppression at the rejection bandwidth. All the aforementioned achievements come at the price of a small reduction in operating bandwidth.

The DGS technique can also be combined with a high impedance thin microstrip line technique in a novel wideband triangle slot antenna. The combined technique provides a strong out-of-band rejection while achieving a very high reduction in size compared to its conventional counterpart antenna. Furthermore, the antenna achieves a very wide band without affecting the gain at 5.8 GHz compared to the conventional triangle slot antenna. The technique used in this triangle slot antenna mitigates the existing issues such as the increase in size, not having enough suppression at the rejection bandwidth, and a reduction in operating bandwidth.

4.1 Introduction

Suppression of the higher order harmonics is of great interest to today's compact communication systems especially for systems with active integrated antennas (AIAs) [90-93]. Since part of the DC power of an active circuit is reflected in high harmonic components, reducing high harmonic components can reduce power wastage and thus, increase power efficiency. Therefore, the antenna should suppress the higher-order harmonics to improve the PAE of the PA in the transmitter [18, 19]. On the receiver side, harmonic suppression is required to cancel out-of-band noise and interference [20-23]. A conventional approach to address these challenges is to use filters in series with the antenna. However, this increases the total size, insertion loss, and implementation cost of the whole system and degrades the noise figure of the receiver. An alternative is to design an antenna with inherent out-of-band rejection capable of rejecting unwanted radiation and suppressing higher-order harmonics. However, most harmonic suppression antennas in the literature did not achieve enough size reduction while having inadequate harmonic suppression.

Furthermore, their harmonic suppression techniques come at the price of reducing operating bandwidth compared to their conventional counterpart antennas.

A metal-insulator-metal (MIM) capacitor, formed by a T-shaped feeding made of a thin microstrip and a grounded stub inside a slot antenna, is previously used to suppress the higher-order out-of-band harmonics [54]. This was achieved without changing the size of the main slot antenna. Another technique in [55] used grounded conductor lines embedded in the dual slot antenna. This antenna creates two resonance frequencies, providing a wide bandwidth. Nevertheless, the design is complicated with many narrow gaps and thin lines, making it prone to manufacturing errors. Furthermore, the fractional bandwidth (FBW) of the antenna is only 18.5%, so it is not suitable for wideband applications. A broadband coplanar waveguide (CPW)-fed loop slot antenna combined with photonic bandgaps (PBGs) of various lattice shapes in the feed network was proposed in [56] for harmonic suppression. However, the PBGs are placed completely outside the antenna, failing to achieve the size reduction goal. In [57], harmonic suppression is achieved using the defected ground slots (DGSs) coupled to the microstrip feed line in a narrowband antenna. A major part of the DGS is placed outside the main radiating slot, leading to an increase in the overall size of the antenna. Moreover, the return loss in the rejection region reaches 2.5 dB, showing inadequate stopband rejection. Other techniques such as the slot coupled filter [58], folded L-shaped slots [59], and stepped impedance slots [60] were used to suppress harmonics without increasing the overall size of the main antenna. However, all these techniques show high return losses and inadequate suppression of higher order resonances in the rejection region. Only the wiggly-line band-stop filter technique [61] achieves good performance in the rejection region, but at the expense of a small operating bandwidth.

In this chapter, first, the two narrow slot antennas, the Double Slot Harmonic Suppression Antenna and the Small Size Slot Harmonic Suppression Antenna, are proposed, all of which use the DGS technique combined with other harmonic suppression techniques. Both the harmonic suppression antennas are developed to work with our 5.8 GHz RFID tag application that uses Amplitude Modulation (AM) with a bandwidth of 200 MHz, which is a narrow bandwidth. The antenna must be compact in size since the size of the RFID tag is small and the requirement of gain is larger than 0 dB. Therefore, the narrow slot structure is chosen for the two antennas because of the small width of the narrow slot. Furthermore, the radiation pattern of the RFID tag is required to be omnidirectional in order to detect a signal in any direction, which is suitable with the radiation pattern of a slot antenna, not the unidirectional radiation pattern of a patch antenna. The gain of a narrow

slot antenna is normally small due to its small aperture, but it still meets the 1dB gain requirement if the size is not too small [94]. The added harmonic suppression structures also reduce the length of both the antennas, compared with their conventional counterpart antennas. Although the bandwidths of the proposed antennas are smaller than their conventional counterpart antennas, they are still bigger than the bandwidth requirement of 200 MHz. Finally, both antennas show a low return loss of 1 to 2 dB at the rejection region, proving they have a very strong rejection capability. This rejection characteristic not also reduces the second and third harmonic components emitted from the RF transceiver, it also rejects any interference other than the operating frequency coming from the outside environment. The length of the Double Slot Harmonic Suppression Antenna is reduced by 8% compared to its conventional counterpart antenna. The length of the Small Size Slot Harmonic Suppression Antenna is reduced by 25% compared to its conventional counterpart antenna.

The two aforementioned narrow slot antennas only work for narrowband applications. For wideband applications, other wideband antenna designs are needed. Therefore, this chapter also describes a wideband triangle slot antenna, named Wideband Triangle Slot Antenna with Out-of-Band Rejection, with out-of-band rejection and a compact size. The antenna covers the whole C-band frequency and sub-6GHz band of 5G. The added harmonic suppression structures significantly improve the bandwidth of the triangle slot antenna. Its size is also reduced by 60% with simple modifications including a simple cutting and a ground reducing technique, thus the proposed antenna can be integrated into portable wideband devices.

Section 4.2 describes the design methodology. Section 4.3 introduces the Double Slot Harmonic Suppression Antenna, while Section 4.4 presents the Small Size Slot Harmonic Suppression Antenna. Finally, in Section 4.5, a wideband triangle-slot antenna, named the Wideband Triangle Slot Antenna with Out-of-Band Rejection, is discussed.

4.2 Design Methodology for Harmonic Suppression Antennas

The design methodology described in this section is derived for the three antennas, the Double Slot Harmonic Suppression Antenna, the Small Size Slot Harmonic Suppression Antenna, and the Wideband Triangle Slot Antenna with Out-of-Band Rejection.

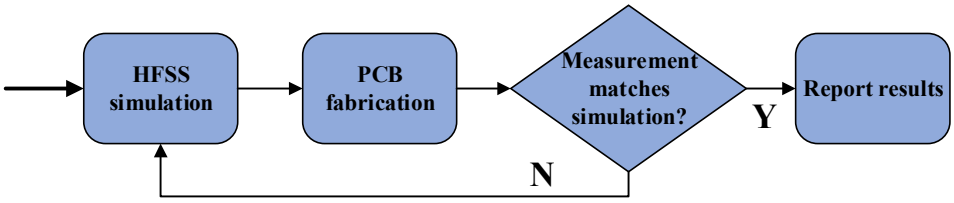


Figure 4-1. Design process for antennas based on HFSS simulation.

Figure 4-1 shows the general design process using simulation. All three antennas are simulated with HFSS, then the Gerber files are extracted and sent to the PCB fabrication company. The PCBs are soldered with SMA connectors. Then, the return loss is measured using a networks analyser and the radiation pattern is measured using anechoic chambers. If the measured results do not match the simulation results within an acceptable deviation, the root causes are sought. Then, other rounds of simulations, fabrications, and measurements are implemented again until the expected results are reached.

Next, the specific design methodology for the three harmonic suppression antennas is described.

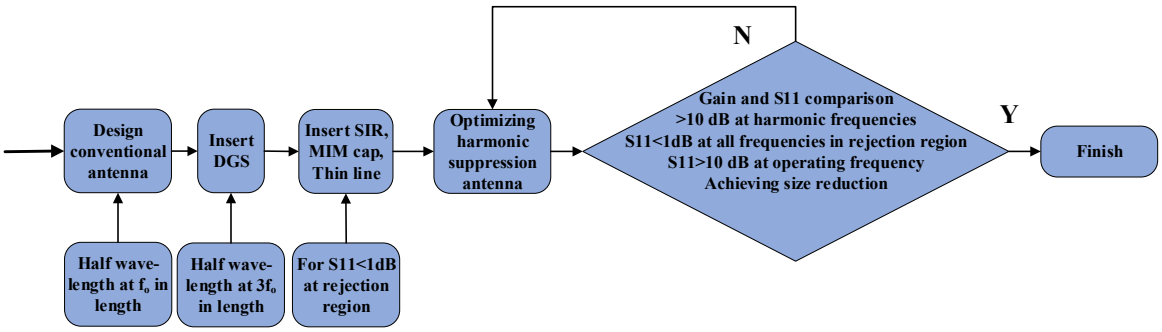


Figure 4-2. Design process in HFSS simulation for the three harmonic suppression antennas. The process begins with designing the conventional antenna.

The process begins with three conventional slot antennas which all have lengths of an effective half-wavelength at 5.8 GHz. The half-wavelength at frequency f_0 is calculated using the following equation:

$$L_s = 0.5\frac{c}{f_0\sqrt{e_{effs}}} \tag{4.1}$$

where e_{effs} (equal to $2e_r/(1+e_r)$) [95] is the effective dielectric constant of the slot and f_0 is the desired frequency, 5.8 GHz.

Then the DGS is inserted inside the slot. The DGS is designed to suppress the third harmonic frequency $3f_0$. Therefore, the initial length of the DGS can be calculated using

equation (4.2) with the frequency of interest $3f_0$. Or the initial length of DGS can be calculated approximately one third of the initial length of the conventional antenna.

The next step is inserting additional harmonic suppression structures such as SIR, MIM cap, and thin line to have S_{11} >1dB at the rejection range. Moreover, these structures are optimized in relation to the bandwidth as well.

The final step is to optimize the harmonic suppression antennas to achieve a gain and S_{11} larger than 10 dB compared to their counterpart conventional antennas. The S_{11} should be larger than 10 dB at the operating frequency and less than 1 dB at the rejection region. The optimization should be implemented in relation to the maximum bandwidth and size reduction as well.

4.3 Double Slot Harmonic Suppression Antenna

This section proposes a double slot harmonic suppression antenna for 5.8 GHz frequency. A simple rectangular DGS is inserted into a conventional rectangular slot antenna to achieve harmonic suppression. It also forms an SIR structure with a natural harmonic suppression characteristic. Furthermore, an MIM capacitor is used as an impedance matching circuit to maintain the bandwidth. The return losses of the antenna at the fundamental and harmonic frequencies are simulated, measured and compared to those of the conventional slot antenna to validate the harmonic suppression performance. The return loss rejection, compared to the conventional antenna, is 3.2 dB at 11.6 GHz and 3.73 dB at 17.4 GHz. The simulated peak gain of the proposed antenna at 5.8 GHz is 0.85 dBi, at 11.6 GHz is -13.2 dBi, and at 17.6 GHz is -13.4 dBi, whereas those of the conventional antenna are 0.74 dBi, -2.44 dBi, and 2.58 dBi, respectively. This means that the radiation pattern suppression is 11 dB and 16 dB at the second and the third harmonic frequencies, respectively, in comparison with the conventional antenna. The bandwidth of the harmonic suppression antenna is 433 MHz or 7.5%, whereas that of the conventional antenna is 577 MHz or 10%, calculated from the operating frequency 5.8 GHz. The length of the harmonic suppression antenna is 8.4% smaller than the conventional slot antenna. The mathematical analysis and an equivalent model are provided to give physical insight into the harmonic suppression mechanism. Based on the author's knowledge, for the first time, the linear relationship between the bandwidth of the SIR slot antenna and its dimension is mathematically derived using transmission line model analysis and is validated using the full wave simulation of HFSS.

4.3.1 Conventional Rectangular Slot Antenna Design

Since an active 5.8 GHz RFID tag has been used as our transceiver, the narrow slot microstrip antenna is chosen over the microstrip patch antenna because it has a very small size and a bandwidth around 10%, calculated from its operating frequency. This configuration is suitable for our RFID tag application which uses amplitude modulation (AM) with a bandwidth of 200 MHz. The slot antenna has an omnidirectional radiation pattern, which can detect an RF signal from any angle, meeting the requirement of the RFID tag application.

The antenna is fabricated on the high frequency substrate Taconic material TLY-5 with 0.5-oz copper, 0.508 mm height, and relative dielectric constant (e_r) of 2.2. The physical parameters of the conventional antenna are listed in Table 4-1.

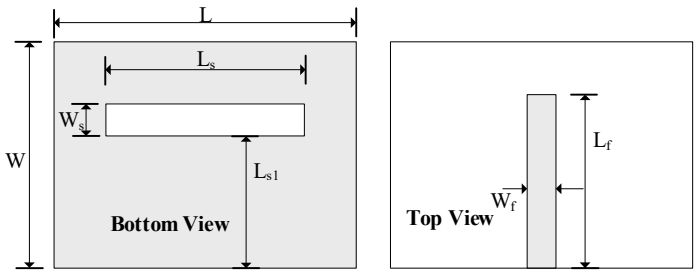


Figure 4-3. The conventional slot antenna with a uniform rectangular shape of slot.

The equivalent circuit of the uniform slot antenna is shown in Figure 4-4 from [96]. The uniform slot can be considered as two lossless short-circuit slot lines with characteristic impedance Z_s and length L_s parallel with a radiation resistor R_A.

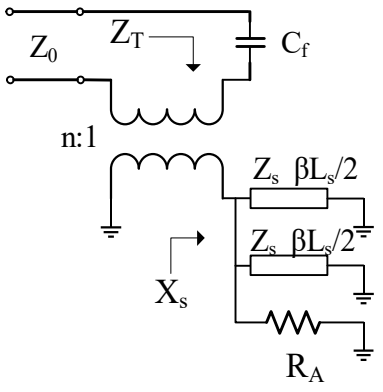


Figure 4-4. Transmission line equivalent circuit of a uniform slot antenna.

The coupling between the microstrip line and the slot lines can be modelled as a power transformer with an ideal turn ratio n:1. The open circuit at the end of the microstrip line is equivalent to a shunt capacitor (C_f).

The reactance of two lossless slot lines can be expressed as:

$$X_s = j\frac{Z_s \tan(\beta L_s/2)}{2} \tag{4.2}$$

The Taylor expression of $\tan(x)$ can be expressed (up to the first three components) as

$$\tan(x) = x + \frac{x^3}{3} + \frac{2x^5}{15} \tag{4.3}$$

Using (4.2) and (4.3), it is obvious that the reactance of a lossless slot line does not have even harmonics (here it is second and fourth harmonics). Therefore, the uniform slot antenna can reject interference until the second harmonic frequency, which is validated by the HFSS simulation and the results are provided later in this section.

In the resonating state of w_0, $X_s = \infty$, leading to $L_s = \frac{\lambda_{effs}}{2}$ while λ_{effs} is the effective wavelength of the slot line. Thus, the initial length of the conventional uniform antenna can be approximately calculated as a half-wavelength as follows:

$$L_s = 0.5\frac{c}{f_0\sqrt{e_{effs}}} \tag{4.4}$$

where e_{effs} (equal to $2e_r/(1+e_r)$) [95] is the effective dielectric constant of the slot and f_0 is the desired frequency, 5.8 GHz. Equation (4.4) considers only the effective dielectric constant and does not consider other parameters such as the width of the slot or the thickness of the substrate. Therefore, further optimizations using simulation software are required to achieve accurate fundamental frequency. After matching optimizations using HFSS simulations for the antenna in Figure 4-3, the length of the slot in the conventional antenna needs to be 16.7 mm, which is ~5 mm different from the calculated value of 22 mm in (4.4).

4.3.2 Harmonic Suppression Antenna Design

This section provides a detailed analysis of the proposed double slot harmonic suppression antenna. First, the geometry and physical parameters of the proposed antenna are introduced. Second, the working principles of the added harmonic suppression structures are explained extensively using mathematical equations and equivalent models. In addition to the harmonic suppression characteristic, the formula of the bandwidth of the proposed antenna is also derived from equivalent circuits. Finally, an MIM cap is used to

neutralize the effect of the added harmonic suppression structures, thus improving the bandwidth.

The proposed harmonic suppression antenna can be broken down into three parts: a) the DGS, b) SIR structures, and c) the MIM cap. The geometry of the proposed antenna is shown in Figure 4-5. The physical parameters of the proposed harmonic suppression antenna are also listed in Table 4-1.

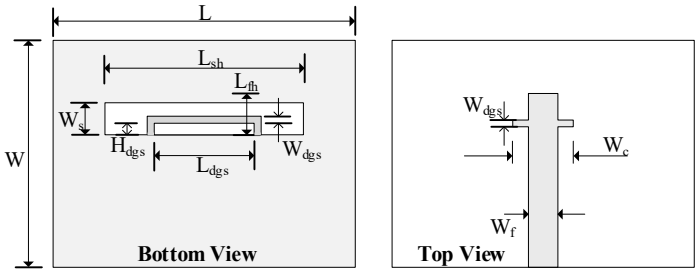


Figure 4-5. The proposed harmonic suppression rectangular slot antenna.

Table 4-1. Physical parameters of the proposed antennas.

Parameters	Values (mm)	Parameters	Values (mm)	Parameters	Values (mm)
h	0.508	W_f	1.56	W_{dgs}	0.5
L	30	L_f	2.3	L_{fh}	2.3
W	30	L_{sh}	15.3	W_c	3.4
L_s	16.7	H_{dgs}	0.55		
W_s	1.5	L_{dgs}	5.4		

4.3.2.1 Defected Ground Slot (DGS)

It is well known that a DGS provides a filter characteristic when coupled with a microstrip line and therefore, can be utilized as a harmonic suppression element in this slot antenna. This section describes the working principle of a rectangular DGS and how it can be integrated into a slot antenna to provide strong rejection across a wide range of frequency which is higher than the operating frequency. It also calculates the initial length of the DGS based on this analysis, which is around one third of the length of the slot antenna.

A rectangular DGS loaded into a microstrip transmission line can be modelled using an equivalent circuit shown in Figure 4-6.

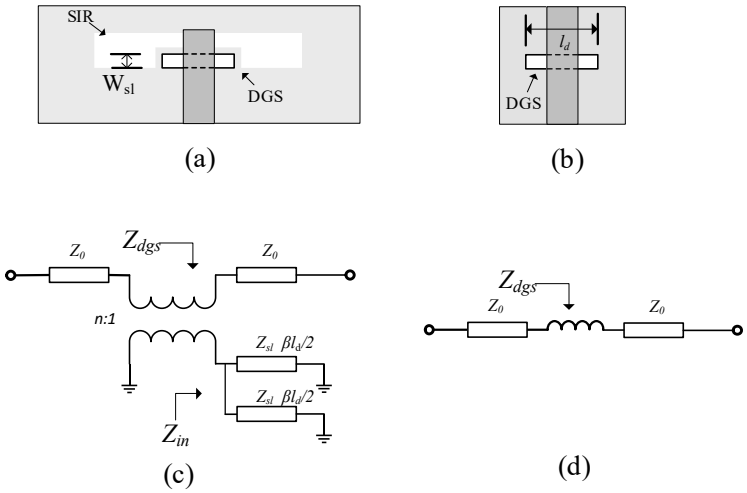


Figure 4-6. Geometry of the DGS inside the rectangular slot antenna and its equivalent circuit. (a) DGS inside the slot antenna, (b) standalone DGS coupled with microstrip line, (c) equivalent circuit of DGS coupled with the microstrip line, (d) DGS can be equivalent to an inductor below its self-resonant frequency of $3f_0$.

In Figure 4-6(c), Z_0 is the characteristic impedance of the microstrip feed line. The coupling between the microstrip transmission line and the DGS is represented by an ideal transformer of n:1 ratio, where n is the coupling factor. The DGS is modelled using a pair of lossless shunt short-circuited slot lines of l_d length. Based on the equivalent circuit, the impedance of the DGS is transformed where Z_{sl} is the characteristic impedance of the DGS slot line, $\beta = 2\pi/\lambda_{\mathrm{effd}}$ is the propagation constant, and λ_{effd} is the effective wavelength of the DGS. The fundamental anti-resonance condition is $Z_{\mathrm{dgs}} = \infty$ resulting in $\tan(\beta l_{\mathrm{d}}/2) = \infty$, leading to $l_{\mathrm{d}} = \lambda_{\mathrm{effd}}/2$. The transmission response of the circuit shows a stopband at this frequency. It is clear that when $0 \leq \beta l_{\mathrm{d}} \leq \pi$, meaning $l_{\mathrm{d}} \leq \lambda_{\mathrm{effd}}/2$, then $\tan(\beta l_{\mathrm{d}}/2) \geq 0$ and Z_{dgs} is inductive. This means that a rectangular DGS acts as a series inductor with a lowpass filtering effect at low frequencies, as shown in Figure 4-6(d). Based on this analysis, the insertion loss of the microstrip-line-coupled DGS is small around the operating frequency of the radiating slot. This ensures a minimal effect of the DGS section on the radiation characteristic of the antenna.

The DGS is designed to have a fundamental anti-resonant frequency at the region of $3*f_0$ to provide a stopband in this region. Therefore, the resonant frequency of DGS is chosen $f_{dgs} = 3 * f_0$ (17.4 GHz) as an initial value. By using (4.4) with the same e_{effs} and from a known L_s , the initial length of the DGS can be calculated equal $\frac{L_s}{(f_{dgs}/f_0)} = 5.6\ mm$.

The Z_{sl} of a slotline can be related to its width as in [97]

$$Z_{sl} = 60 + 3.69\sin\left(\frac{(\mathrm{e}_r - 2.22)\pi}{2.36}\right) + 133.5\ln(10\mathrm{e}_r)\sqrt{\frac{W_{sl}}{\lambda_0}}$$
$$+ 2.81[1 - 0.011\mathrm{e}_r(4.48 + ln\mathrm{e}_r)]\left(\frac{W_{sl}}{h}\right)\ ln\left(\frac{10h}{\lambda_0}\right)$$
$$+131.1(1.028 - ln\mathrm{e}_r)\sqrt{\frac{h}{\lambda_0}} \qquad (4.5)$$
$$+ 12.48(1 + 0.18ln\mathrm{e}_r)\frac{W_{sl}/h}{\sqrt{\mathrm{e}_r - 2.06 + 0.85(W_{sl}/h)^2}}$$

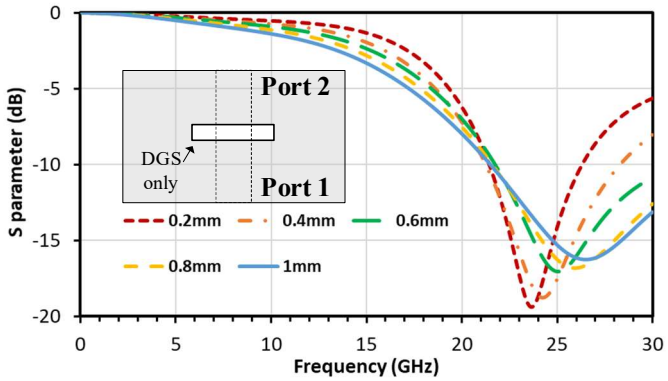


Figure 4-7. Insertion loss of DGS only when changing its width, W_{sl}. Its length equals L_{dgs} which is 5.4 mm.

where W_{sl} is the width of the slot (here H_{dgs}), and h is the thickness of the substrate. λ_0 is the free space wavelength. The equation is only applied with the condition $0.006 \leq \frac{h}{\lambda_0} \leq 0.060$ (where h =0.508 mm), $0.0015 \leq \frac{W_{sl}}{\lambda_0} \leq 0.075$ (therefore W_{sl} is from 0.0775 mm to 3.88 mm), and $2.2 \leq \mathrm{e}_r \leq 3.8$ (where $e_r = 2.2$). The condition is based on the assumption of the uniform electrical field in a slot and the condition of least-square curve fitting. From Figure 4-7, it is obvious that the bigger W_{sl}, meaning the wider the slot line, the bigger the Z_{sl}, hence, the better the harmonic suppression. The simulation insertion loss of DGS with several width values can be seen in Figure 4-7. It is obvious that the higher insertion loss of the bigger W_{sl} may affect the low frequency region of the slot antenna. Moreover, the big inductance of DGS, thus the large width, can affect the bandwidth of the slot antenna (explained in the next section). Therefore, width W_{sl} must be chosen at a

balance point of harmonic suppression, resonant frequency and bandwidth. The width of DGS is chosen initially to equal W_s /3, 0.5 mm for simplicity.

After optimization using HFSS in consideration of the harmonic suppression, resonant frequency, and bandwidth of the slot antenna, its length L_{dgs} is 5.4 mm and its height H_{dgs} is 0.55 mm. By observing the simulated insertion loss of the DGS-only structure in Figure 4-7, a stop band begins to appear at the region of the third harmonic. Furthermore, the DGS slightly improves impedance matching, thus widening the bandwidth of the SIR-only slot antenna from 300 MHz to 330 MHz, as shown in the inset of Figure 4-8. Therefore, a DGS can be used as both an impedance matching circuit and a harmonic suppression circuit.

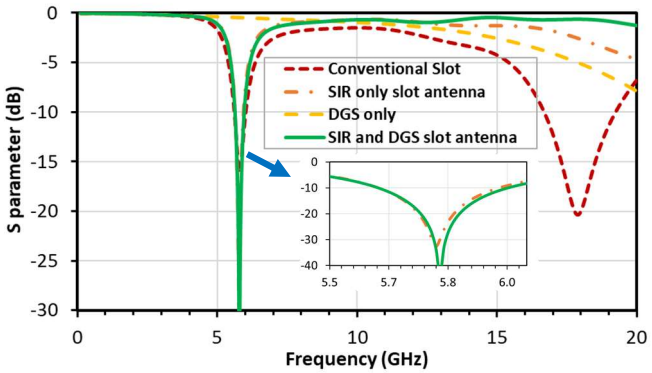


Figure 4-8. Impact of DGS to return loss of the SIR slot antenna.

4.3.2.2 Stepped Impedance Resonator (SIR)

The shape of the DGS structure, when inserted entirely into a rectangular slot, changes the rectangular slot into a stepped-impedance resonator (SIR) structure as shown in Figure 4-9 , which has a natural harmonic suppression property.

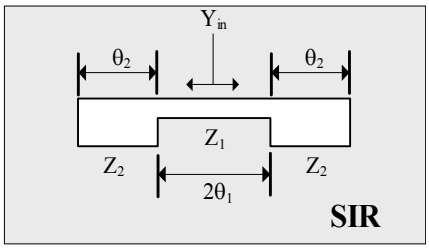


Figure 4-9. Geometry of the SIR.

The harmonic suppression and size reduction mechanism of the SIR slot in Figure 4-9 are described in [96]. Ignoring the influence of step discontinuity, the input admittance of the SIR slot can be expressed using the transmission line impedance formula as

$$Y_{in} = \frac{1}{Z_{in}} = j2Y_1 \frac{K\,tan\theta_1 tan\theta_2 - 1}{tan\theta_1 + Ktan\theta_2} \tag{4.6}$$

where the impedance ratio $K = Z_2/Z_1$ and $Y_1=1/Z_1$. θ_1 and θ_2 are the electrical length of the two slotlines. The fundamental resonance condition occurs when $Y_{in} = 0$ with the satisfied boundary condition, thus, $K\,tan\theta_1 tan\theta_2 - 1 = 0$. From this equation and by letting K=1, the length of a uniform slot (see Figure 4-3) can be calculated, which is $2\theta_1 + 2\theta_2 = \pi$ and thus, is equal to half an effective wavelength, matching equation (4.4).

With the assumption that $\theta_1 = \theta_2$ for easy calculation and to solve $K\,tan\theta_1 tan\theta_2 - 1 = 0$ with K≠ 1, the first or smallest harmonic of the SIR structure can be calculated:

$$f_{s1} = f_0 \left(\frac{\pi}{\arctan\left(\frac{1}{\sqrt{K}}\right)} - 1 \right) \tag{4.7}$$

In the case of a uniform slot (K=1), the smallest harmonic frequency $f_{s1} = 3f_0$ and it is the third harmonic of the transceiver. Therefore, the second harmonic $(2f_0)$ of the uniform slot does not exist. In the case of an SIR slot and $K > 1$, f_{s1} is bigger than $3f_0$, hence it reflects some power from the third harmonic of the transceiver and rejects $3f_0$ interference. The SIR slot does not have the second harmonic $(2f_0)$ as well since the smallest harmonic frequency is bigger than $3f_0$. Therefore, the SIR slot with $K > 1$ not only reduces the size of the antenna below half an effective wavelength, it can also suppress the third harmonic.

From [97], the impedance Z_1, having the narrower width $W=W_s-H_{dgs}-W_{dgs}$, can be calculated to be equal to 117 Ω which is smaller than impedance Z2, 139 Ω (4.5), with wider width $W=W_s$, resulting in K=1.19 > 1.

To calculate the total length of the proposed antenna, the antenna fundamental frequency formula in [96] is used with the assumption that $\theta_1 = \theta_2$:

$$f_0 = 2\left(\frac{c}{L_{sl}\pi\sqrt{e_{effs}}} \arctan\left(\frac{1}{\sqrt{K}}\right) \right) \tag{4.8}$$

where L_{sl} is the total length of the slot.

As the fundamental frequencies for both conventional (K=1) and the proposed antenna (K=1.19) are the same, L_{sh} is calculated from (4.7), $L_{sh} = \left(\frac{4L_s}{\pi}\right)\arctan\left(\frac{1}{\sqrt{K}}\right)$ for the proposed harmonic suppression antenna. With $L_s=16.7$ mm, L_{sh} will be equal to 15.77 mm. However, the width $\theta_1 \neq \theta_2$ due to the fact that $\theta_2 \sim 2\theta_1$ which is approximately the length of DGS (which is around one third of the total slot antenna) and discontinuities, L_{sh} is optimized to 15.3 mm using simulations, which is 8.3% shorter than length L_s of the

conventional antenna. In other words, the two steps in the SIR structure lengthen the route of the surface current running along the edge of the slot, thus, a smaller-sized slot can be achieved.

Using equation (4.8), $3.23*f_0$ is used for the third harmonic of the proposed antenna, which is outside the transceiver's third harmonic frequency. In other words, the SIR shifts its third harmonic resonance frequency out of the exact third harmonic frequency. As a result, the third harmonic frequency of the transceiver does not pass through the proposed antenna. The simulated return loss of the conventional slot antenna is compared to the SIR structure in Figure 4-8. As expected, by using the SIR structure, the third harmonic is suppressed around 14 dB.

When K is increased by reducing Z_1 using a narrower slot, the third harmonic will be shifted to the higher frequency, meaning the SIR slot has a stronger harmonic suppression capability. However, by narrowing Z_1, the bandwidth of the slot antenna greatly decreases, which is proven using mathematical equations in the next section.

4.3.2.3 Bandwidth of SIR

In this section, the relationship between the bandwidth of an SIR structure and its impedance components, including Z_1 and Z_2, is analysed using a mixed model of equivalent lumped circuits and transmission line model. This model can be used to predict the trend of the bandwidth when altering the widths of the two impedance lines, and thus impedance Z_1 and Z_2 and impedance ratio K of an SIR structure.

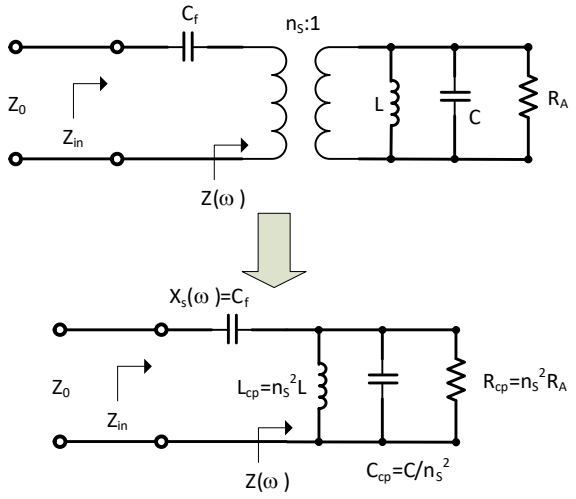


Figure 4-10. Lumped-element equivalent circuit of the SIR antenna and its corresponding circuit without a transformer.

Figure 4-10 shows a lumped-element equivalent circuit of the SIR antenna on the top and its derived version on the bottom. On the top of Figure 4-10, the slot antenna can be expressed as a lumped-element parallel-resonance circuit consisting of L, C, R_A, C_f with an ideal transformer with ratio n_S:1 [96]. However, corresponding circuit without a transformer can be derived as shown on the bottom of Figure 4-10 in order to calculate its quality factor and bandwidth [98] as follows:

$$Z_{in} = -j\frac{1}{\omega C_f} + {n_S}^2 \frac{1}{\frac{1}{R_A} + j\omega C - j\frac{1}{\omega L}} \tag{4.9}$$

$$= -j\frac{1}{\omega C_f} + \frac{1}{\frac{1}{{n_S}^2 R_A} + j\omega\frac{C}{{n_S}^2} - j\frac{1}{\omega {n_S}^2 L}}$$

where the parallel capacitance C can be calculated [96]

$$C = \frac{L_{sh}}{2 v_p Z_1} \tag{4.10}$$

where v_p is the phase velocity of the wave in the slot line.

$$v_p = \frac{2c}{\sqrt{\mathrm{e}_{effs}}} \tag{4.11}$$

Therefore, from (4.9), (4.10) and [98]-D.16 the quality factor of the SIR antenna can be calculated as:

$$Q = \omega_0 R_{pc} C_{pc} = \omega_0 (C/n^2)(R_A n^2) = \omega_0 C R_A \tag{4.12}$$

$$= \frac{R_A \omega_0 L_{sh}}{2\, v_p\, Z_1} = \frac{K R_A \omega_0 L_{sh}}{2\, v_p\, Z_2}$$

Using (4.4) and (4.11) to (4.12)

$$Q = \frac{\pi K R_A f_0}{4\ Z_2} \tag{4.13}$$

The fractional matched voltage-standing-wave-ratio (VSWR) bandwidth, $FBW_v(\omega_0)$, for the SIR antenna at a frequency ω_0 is defined as the difference between the two frequencies on either side of ω_0, meaning ω_+ and ω_-, at which the VSWR equals a constant s, divides to ω_0. For example, at -10 dB bandwidth using return loss S_{11}, VSWR =s= 1.92. The fractional matched VSWR bandwidth with -10 dB return loss (bandwidth) will be calculated using equation (41) in [98]- as

$$FBW_v(\omega_0) = \frac{\omega_+ - \omega_-}{\omega_0} \approx 2\frac{\sqrt{\beta}}{Q} = 8\frac{\sqrt{\beta}}{\pi}\frac{Z_2}{KR_A f_0} \quad (4.14)$$

where $\sqrt{\beta} = \frac{s-1}{2\sqrt{s}} = 0.33$ (at s= $S_{11} = -10\ dB$).

In equation (4.14), the transmission line model is employed to calculate (4.10). Although this model is not very accurate because it does not consider parasitic resistance and inductance at the short circuit and capacitance at discontinuities, it provides the intuition necessary to understand the relationship between the bandwidth of an SIR slot antenna with its slot line impedance and impedance ratio K. In the case of a uniform slot antenna (K=1), it is obvious that $FBW_v(\omega_0)$ at resonant frequency ω_0, is linearly proportional with Z_2.

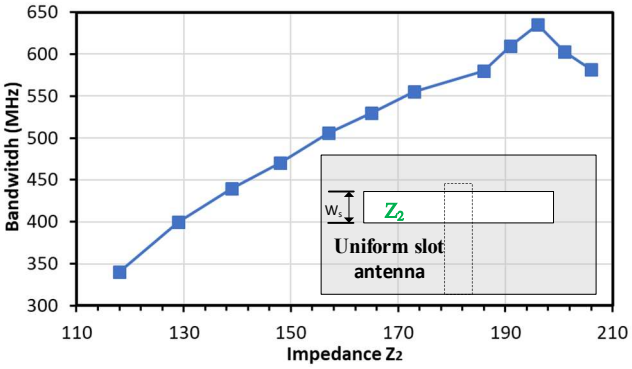


Figure 4-11. Relationship between the bandwidth of a uniform slot antenna and the impedance of its slot line (Z_2). The resonant frequency is at 5.8 GHz.

From [97], it is clear that the wider the slot, the larger the characteristic impedance Z_2. Hence, the wider the slot, the wider the bandwidth of the slot. This relationship can be validated by HFSS simulation and is shown in Figure 4-11, Figure 4-12, and Figure 4-13.

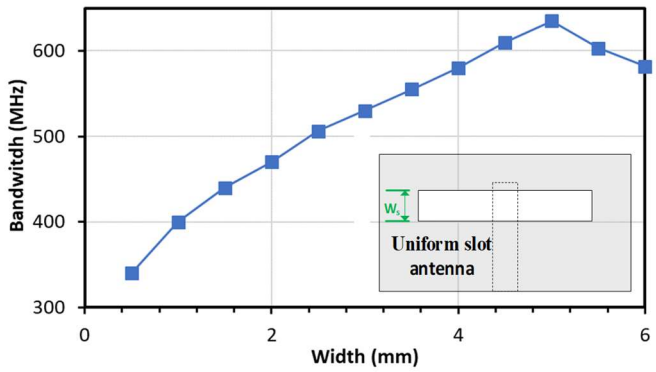


Figure 4-12. Relationship between the bandwidth of a uniform slot antenna with the width of the slot. The resonant frequency is at 5.8 GHz.

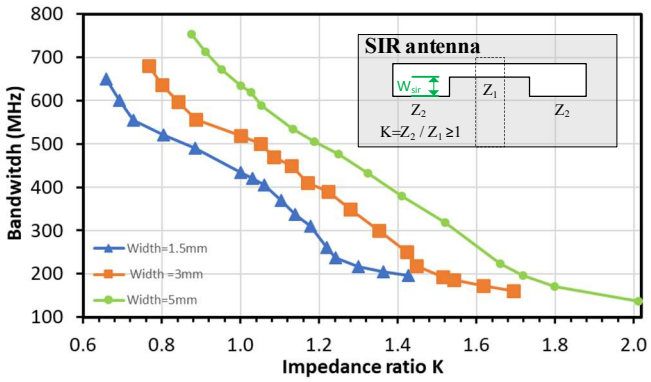


Figure 4-13. Relationship between the bandwidth of an SIR slot antenna and the impedance ratio K (K≥1). The width of the slot antenna (Z_2), W_s, is 1.5 mm, 3 mm and 5 mm. The resonant frequency is at 5.8 GHz.

Figure 4-11 also shows the linear relationship between the impedance of the slot line and the bandwidth of an uniform slot antenna, which is proven by (4.14). Figure 4-12 shows the relationship between the width of a slot line and its bandwidth for dimension-bandwidth visuality. This relationship is also almost linear because the impedance of the slot line, calculated by (4.6), is also in an almost linear relationship with its width in narrow slots [97] . It is observed from Figure 4-11 and Figure 4-12 that from the width 5mm of the slot, the bandwidth does not keep a linear relationship with impedance Z_2 and the width of the slot. This is because the transmission line model, which is used to calculate capacitance C in (4.10), assumes that the slot line ends with two ideal short circuits to the ground as in Figure 4-6. However, it is only valid when the width of the slot line is small enough. When the width is bigger than a certain value where the parasitic resistance and inductance at short circuits cannot be ignored , the two short circuits must be replaced by an LR circuit, where L is the equivalent inductance and R represents the loss through it [99]. Both L and R are dimension- and frequency-dependent, therefore they can distort the linear relationship.

Furthermore, the relationship between the bandwidth and width of the slot is validated experimentally in [100] with two samples of widths. The bigger the width, the bigger the bandwidth.

In the case of the SIR slot antenna (K>1) with a fixed Z_2, the bandwidth is inversely proportional with K. The relationship between bandwidth and impedance ratio K is also represented by equation (4.14). It is obvious that the bigger the K, the smaller the bandwidth. This relationship is validated using the full wave analysis of HFSS software. The simulation results are shown in Figure 4-13. It is observed that the bandwidth is an inverted linear function of K with a low value. At a higher value of K, which is 1.22, 1.45

and 1.72 where the width is 1.5, 3 and 5 mm, respectively, the bandwidth does not keep the linear rule. This is where the width of Z_1 all equals to 0.3mm, meaning a small microstrip gap. This microstrip gap can be represented by equivalent capacitances [101]. These caps, which are dimension- and frequency-dependent, contribute to the cap value of (4.10) and alter the linear relationship between the bandwidth and K.

In conclusion, a value of K must be chosen to balance between the bandwidth goal and the harmonic suppression goal. The higher the K value, the better the harmonic suppression capability, because the third harmonic frequency is shifted to a higher frequency. The length of the slot antenna is also shorter because the surface current must travel along a bigger step. However, these advantages come at the price of narrower bandwidth.

4.3.2.4 MIM Cap

Because the DGS has an inductive property below $3f_0$ as stated in section 4.3.2.1, a capacitor is needed to neutralize this inductance to obtain a wider bandwidth at resonant frequency f_0. Therefore, a MIM cap shown in Figure 4-14 is introduced right after the DGS.

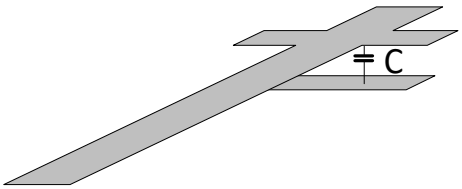


Figure 4-14. Geometry of the MIM cap.

The MIM cap value can be calculated as follows:

$$C_{MIM} = \mathrm{e}_r \mathrm{e}_o \frac{A}{h} \tag{4.15}$$

where e_r is the relative permittivity or dielectric constant of the insulator (2.2 in the TLY-5 substrate), e_o is the absolute permittivity of the vacuum, which is 8.85x10-12 F/m. A is the area of the MIM cap which is *Wc* x *Wdgs* (see Figure 4-5). Finally, *h* is the plate distance or thickness of the substrate equal to 0.508 mm. Therefore, C_{MIM} = 65 fF. The value of this capacitor is small enough not to shift to the resonant frequency.

By comparing the return simulated loss of the slot antenna with and without the MIM cap in Figure 4-15, the contribution to harmonics suppression of the MIM cap is negligible. However, as Figure 4-15 suggests, the MIM cap helps widen the bandwidth at -10 dB from 330 MHz to 360 MHz.

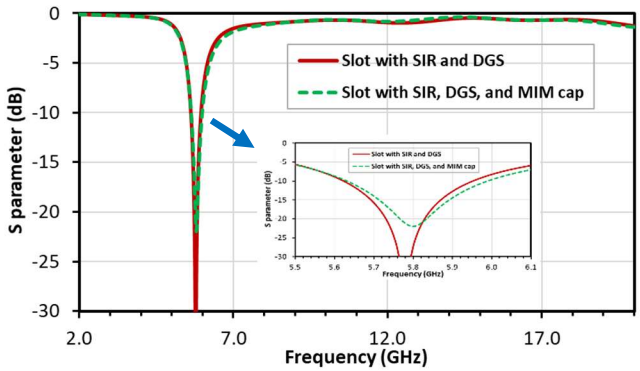


Figure 4-15. Simulated return losses of slots with and without the MIM cap.

4.3.3 Simulation and Measurement Results

As previously mentioned, both the conventional antenna in Figure 4-3 and harmonic suppression antenna in Figure 4-5 were manufactured using Taconic material substrate TLY-5. The front and back views of both the fabricated prototypes are presented in Figure 4-16. The length of the harmonic suppression slot antenna is 8.4% smaller than the conventional slot antenna.

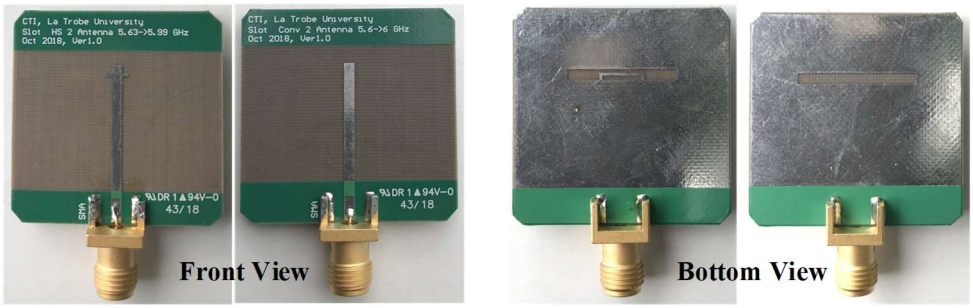


Figure 4-16. Photograph of the fabricated antennas. The proposed antenna is on the left side of each photo, whereas the conventional triangle slot antenna is on the right.

The return loss measurements using Network Analyser Anritsu 37377C are shown in Figure 4-17 together with the simulation results from the ANSYS HFSS software. The conventional slot antenna has a bandwidth of 577 MHz (10%) and the harmonics supersession antenna has a bandwidth of 433 MHz (7.5%) with the centre frequency of 5.8 GHz. At the second harmonic suppression frequency, the return loss of the proposed antenna is 0.6 dB while that of the conventional antenna is 3.8 dB. At the third harmonic frequency, the return loss of the proposed antenna is 1.67dB while that of the conventional antenna is 5.4 dB. This means that the proposed antenna provides 3.2 dB suppression in

return loss at the second harmonic frequency and 3.73 dB in return loss at the third harmonic frequency.

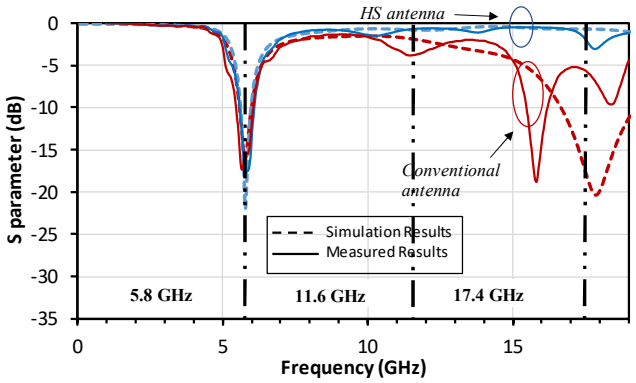


Figure 4-17. The simulated and measured return losses of the proposed antennas. The harmonic suppression antenna has low return loss at the second and the third harmonic frequencies, compared to the conventional antenna.

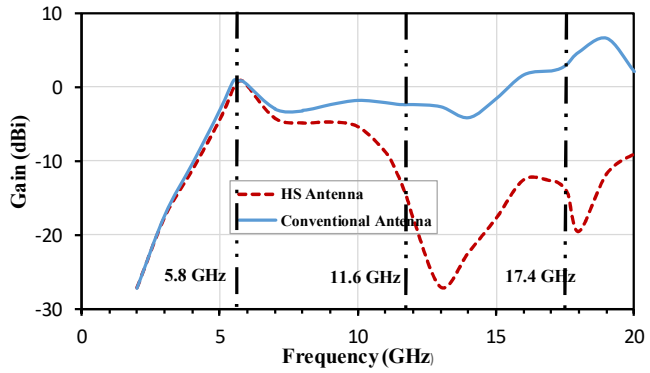


Figure 4-18. Simulated gain in HFSS of the conventional and proposed antennas. The harmonic suppression antenna has low gain at the second and the third harmonic frequencies, compared to the conventional antenna.

The broadside gains across frequencies from 2 GHz to 20 GHz of the conventional antenna and the proposed antenna are simulated using HFSS and shown in Figure 4-18. It can be observed that the simulated gains at the fundamental frequency of the harmonic suppression antenna is 0.85 dBi while that of the conventional antenna is 0.74 dBi. The simulated gains of the harmonic supersession antenna at the second and the third harmonic frequencies are -13.2 and -13.4 dBi, respectively, whereas those of the conventional antenna are -2.44 and 2.58 dBi, respectively. The gains are recorded at the broadside of both the antennas. This means the proposed antenna provides about 11 dB suppression at the second and 16 dB at the third harmonic frequencies in the radiation pattern.

Next, the radiation patterns of both antennas at the fundamental frequency are simulated and shown in Figure 4-19. The co-polarization radiation patterns of both antennas at the fundamental frequency are similar to each other and comparable to a simple slot antenna. This means that the added harmonic suppression structures and the MIM cap do not alter the gain and radiation pattern at the fundamental frequency.

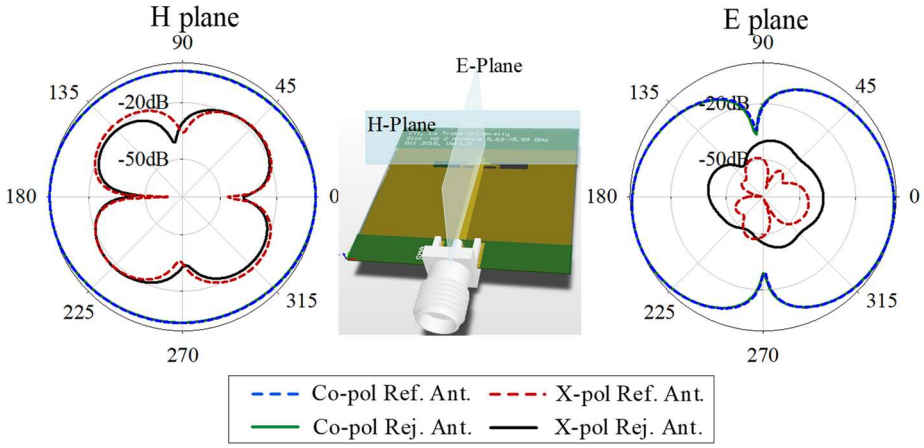


Figure 4-19. Comparison of simulated radiation patterns of the proposed antennas at 5.8 GHz.

4.3.4 Summary

In this work, a double slot antenna with harmonic suppression characteristic over the second and third harmonic frequencies was proposed. The return loss was very high from 7 GHz to 20 GHz, including the second and third harmonic frequencies, showing a strong rejection capability. Furthermore, the length of the harmonic suppression antenna reduces by 8.4% compared to the conventional antenna, with only a 2.5% reduction in operating bandwidth. The geometry of the proposed antenna is simple with two rectangular slots. The design process is straightforward with the half-wavelength slot antenna and one-sixth wavelength DGS. Therefore, the optimization time is short. Furthermore, the size of the proposed antenna is 0.36 x 0.034 (wavelength x wavelength) which is very small. However, if a further size reduction in the length of the antenna is needed, another technique is required. The next section presents another harmonic suppression slot antenna, which has the size of 0.27 x 0.065 (wavelength x wavelength). This means that it is possible to achieve a further 25% (= (0.36-0.27)/0.36) length reduction.

4.4 A Small-Size Slot Harmonic Suppression Antenna

This section proposes a small size meander slot harmonic suppression antenna for 5.8 GHz frequency. A hairpin-like structure, which is inserted into a conventional rectangular slot, is used to achieve harmonic suppression. The hairpin-like structure creates a stepped-

impedance resonator (SIR) slot antenna, which has a natural harmonic suppression characteristic. It also creates a dumbbell defected ground slot (DGS) that helps suppress the third harmonic. Moreover, a narrow microstrip line is inserted within the hairpin to reduce the size of the antenna further and provide a greater harmonic suppression capability. The return loss and radiation pattern of the antenna at the fundamental and harmonic frequencies are measured and compared to those of the conventional slot antenna to validate the harmonic suppression performance. The rejection is 4.8 dB at 11.6 GHz and 5.8 dB at 17.4 GHz. In addition to harmonic frequencies, the proposed antenna can reject all out-of-band frequencies due to very low return loss across the whole range of the out-of-band frequency. The 10-dB return loss bandwidth of the harmonic suppression antenna is 320 MHz (5.5%), while that of the conventional antenna is 580 MHz (10.2%). The peak gain of the proposed antenna at 5.8 GHz is 0.1 dBi, at 11.6 GHz is -20.4 dBi, and at 17.6 GHz is -21.8 dBi while those of the conventional antenna are 0.55 dBi, -0.4 dBi, and 4.2 dBi, respectively. This means the proposed antenna provides about 21 dB suppression at the second and 16.6 dB at the third harmonic frequencies in the radiation pattern. Moreover, the size of the harmonic suppression antenna is 25% smaller than the conventional rectangular antenna. Mathematical analysis is provided to give physical insight into the harmonic suppression mechanism.

4.4.1 Harmonic Suppression Analysis

Since an active 5.8 GHz RFID tag is used as our transceiver, the narrow slot microstrip antenna is chosen because it has a very small size and a bandwidth of around 10%, calculated from its operating frequency. This configuration is suitable for our RFID tag application that uses Amplitude Modulation (AM) with a bandwidth of 200 MHz, and the omnidirectional radiation pattern compulsory for our used case.

The proposed antenna (see Figure 4-21) was manufactured together with a conventional rectangular slot antenna for comparison purposes (see Figure 4-20). The working principles of the conventional rectangular slot antenna can be seen in section 4.3.1. After performing optimisations using HFSS simulations for the antenna in Fig. 1 (a), the length of slot L_s in the conventional antenna needs to be 15.7 mm, which is ~6 mm different from the calculated value of 22 mm using (4.4). The length of slot L_s is 1 mm larger than the previous antenna in section 4.3.1 because the current width W_s is 2.9 mm, which is larger than the previous width W_s of 1.5 mm. The current width W_s is larger for a better bandwidth and for the insertion of the bigger harmonic suppression structure.

The proposed harmonic suppression antenna with a hair-pin like structure is inserted inside the main radiating slot is described in Figure 4-21. These antennas are fabricated on the high frequency substrate Taconic material TLY-5 with 0.5-oz copper, 0.508 mm height, and relative dielectric constant (e_r) of 2.2. The physical parameters of both the proposed antennas are listed in Table 4-2.

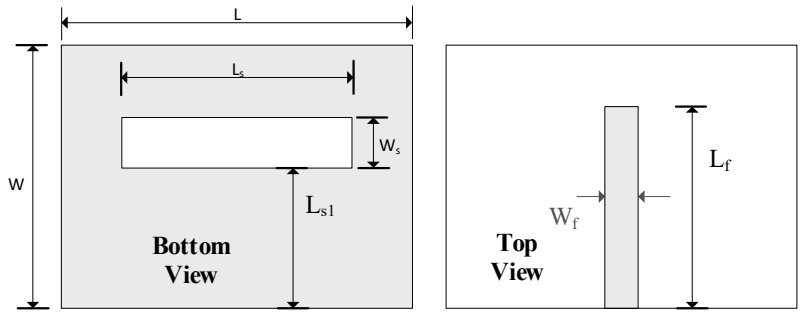


Figure 4-20. The conventional slot antenna.

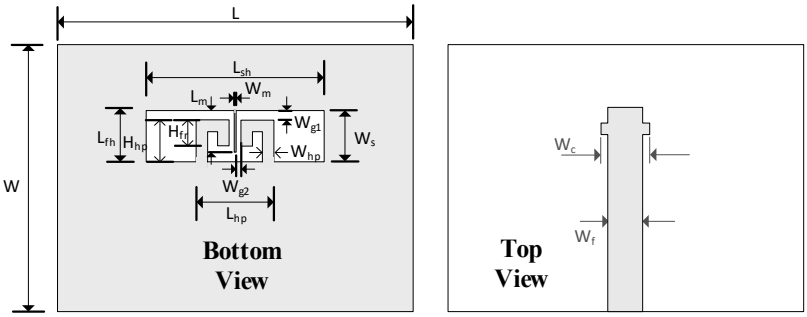


Figure 4-21. The proposed harmonic suppression antenna.

Table 4-2. Physical parameters of the proposed antennas

Parameters	Values (mm)	Parameters	Values (mm)	Parameters	Values (mm)
h	0.508	L_f	3.3	W_{g1}	0.7
L	30	L_{sh}	11.8	W_{g2}	0.225
W	30	H_{hp}	2.2	W_m	0.15
L_s	15.7	L_{hp}	3.6	L_m	2.5
W_s	2.9	W_{hp}	0.5	H_{fr}	1.3
W_f	1.56	L_{fh}	3		

The shape of the hairpin-like structure is designed to change the rectangular slot into an SIR structure, which has a natural harmonic suppression property. It also creates a dumbbell DGS, which has a filter property. Finally, a narrow meander line is inserted between the hairpin structures to create fringing capacitors and reduce size. Hence, the

proposed harmonic suppression antenna can be broken down into three parts for analysis: a) the SIR structure, b) the DGS, and c) fringing capacitors and meander line as illustrated in Figure 4-22.

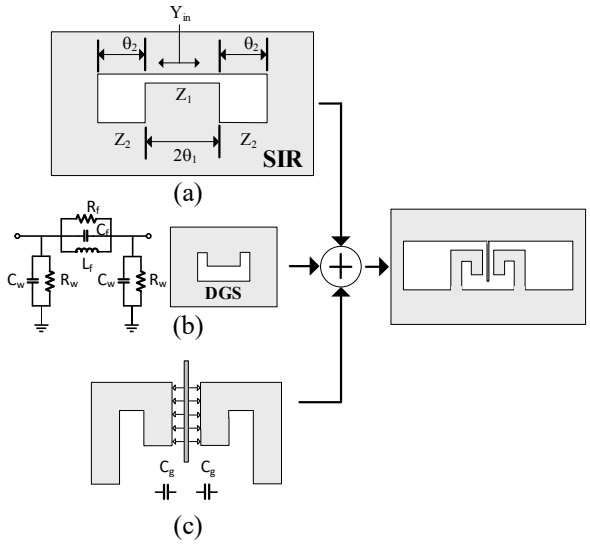


Figure 4-22. (a) Geometry of the SIR, (b) geometry of the DGS and its equivalent circuit, (c) geometry of the fringing capacitance and meander line.

As seen in Figure 4-22 (b), the dumbbell DGS is used as a low pass filter. Its working principle can be seen in section 4.3.2.1. By observing the simulated insertion loss using HFSS software of the DGS structure in Figure 4-23 (DGS only), a small stop band begins to appear at the region of the third harmonics.

The harmonic suppression and size reduction mechanism of the SIR slot in Figure 4-22 (a) are described in section 4.3.2.1. The simulated return loss of the conventional rectangular slot antenna is compared to the SIR slot structure in Figure 4-23. As expected, by using the SIR structure, the third harmonic is suppressed by about -14 dB.

The fringing cap value, which is due to fringing fields in the gap between the meander line and the hairpin structure as shown in Figure 4-22 (c), can be expressed [102] as follows:

$$C_g = \mathrm{e}_e \frac{tH_{fr}}{W_{g2}} + \mathrm{e}_e(t + H_{fr} + W_{g2}) \tag{4.16}$$

where $e_e = e_o(1 + e_r)/2$ is the effective permittivity or dielectric constant of the insulator, e_o is the absolute permittivity of vacuum equal to 8.85×10^{-12} F/m. H_{fr} is the length of the portion of the hairpin which is in the fringing fields with the meander line. t is the thickness of the substrate copper (0.5 oz or 17.5 µm). Therefore, based on (4.16), *Cg = 21.8 fF*.

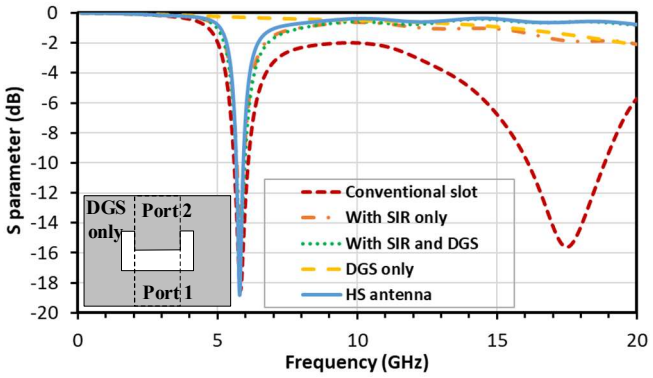


Figure 4-23. Simulated return loss of slots with and without SIR and DGS, and simulated insertion loss of the DGS only (the geometry is in the bottom left corner).

By comparing the return losses of the slot antenna with and without the meander line in Figure 4-24, it is clear that the fringing caps slightly contribute to harmonic suppression, especially at the second harmonic frequency region due to narrowing the operating bandwidth. Furthermore, the meander line also reduces the length of the harmonic suppression antenna from 14.6 mm to 11.8 mm, or 19% (= (14.6-11.8)/14.6) by forming a single meander section slot with the hairpin. The surface current needs to travel through this section, thus enlarging the effective length. Therefore, by combining SIR, the hairpin, and meander line, the total size of the harmonic suppression antenna reduces greatly compared to the size of the conventional slot antenna.

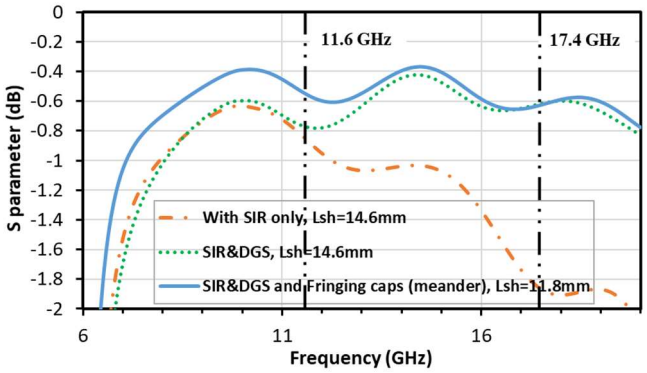


Figure 4-24. Simulated return losses of slots from 10 GHz to 20 GHz.

4.4.2 Simulation and Measurement Results

As previously discussed, both the conventional antenna in Figure 4-20 and the harmonic suppression antenna in Figure 4-21 were manufactured using Taconic material

substrate TLY-5. The front and back views of both the fabricated prototypes are presented in Figure 4-25.

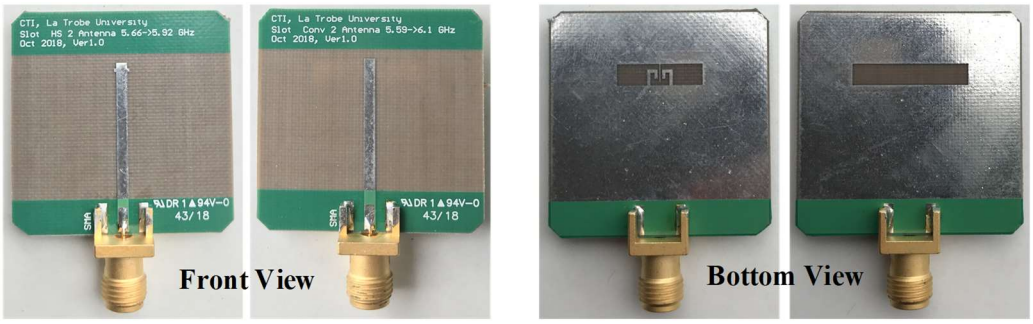


Figure 4-25. Photograph of the fabricated antennas. The proposed antenna is on the left side of each photo, whereas the conventional triangle slot antenna is on the right.

The return loss measurements using Network Analyser Anritsu MS4644B are shown in together with the simulation results from the ANSYS HFSS software. The conventional slot antenna has 10 dB return loss from 5.5 to 6.08 GHz, meaning a bandwidth of 580 MHz (10.2%) when calculated from the desired frequency 5.8 GHz. The harmonic supersession antenna has 10 dB return loss from 5.72 to 6.05 GHz, meaning a bandwidth of 330 MHz (5.7%). The resonant frequency of the conventional antenna is 5.885 GHz whereas that of the proposed antenna is 5.95 GHz. The discrepancy between the simulation and the measured results is due to PCB manufacturing variations, SMA connector discontinuity and substrate imperfection. Despite these variations, the return loss performance for our industrial project is still acceptable because the required frequency 5.8 GHz is still in the 10 dB bandwidth. The measured return loss is very high at the second and third harmonic frequencies, 0.53 dB and 0.75 dB respectively, compared to the

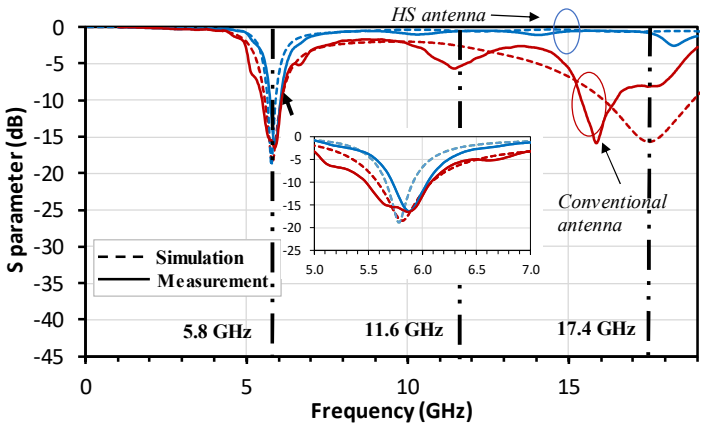


Figure 4-26. The simulated and measured return losses of the proposed antennas.

conventional slot antenna, 5.4 dB and 8.12 dB, respectively. This means that the proposed antenna provides 4.87 dB suppression in return loss at the second harmonic frequency and 7.37 dB in return loss at the third harmonic frequency.

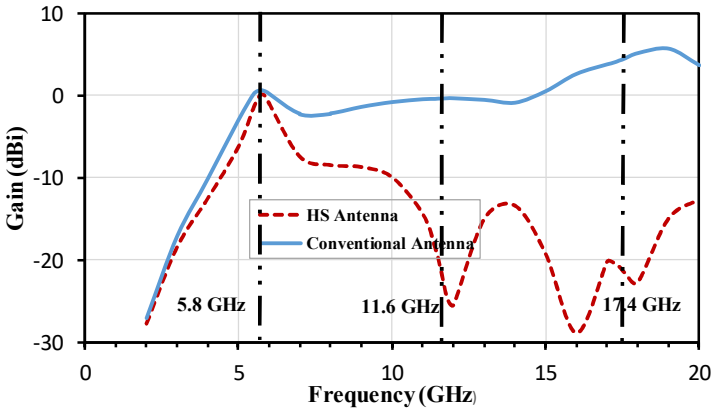


Figure 4-27. Simulated gain in HFSS of the conventional and proposed antennas.

The broadside gains across frequencies from 2 GHz to 20 GHz of the conventional antenna and the proposed antenna are simulated using HFSS and shown in Figure 4-27. It can be observed that the simulated gains at the fundamental frequency of the harmonic suppression antenna is 0.1 dBi while that of the conventional antenna is 0.55 dBi. The simulated gains of the harmonic supersession antenna at the second and the third harmonic frequencies are -21.4 and -20.8 dBi, respectively, whereas those of the conventional antenna are -0.4 and 4.2 dBi, respectively. The gains are recorded at the broadside of both the antennas. This means the proposed antenna provides about 21 dB suppression at the

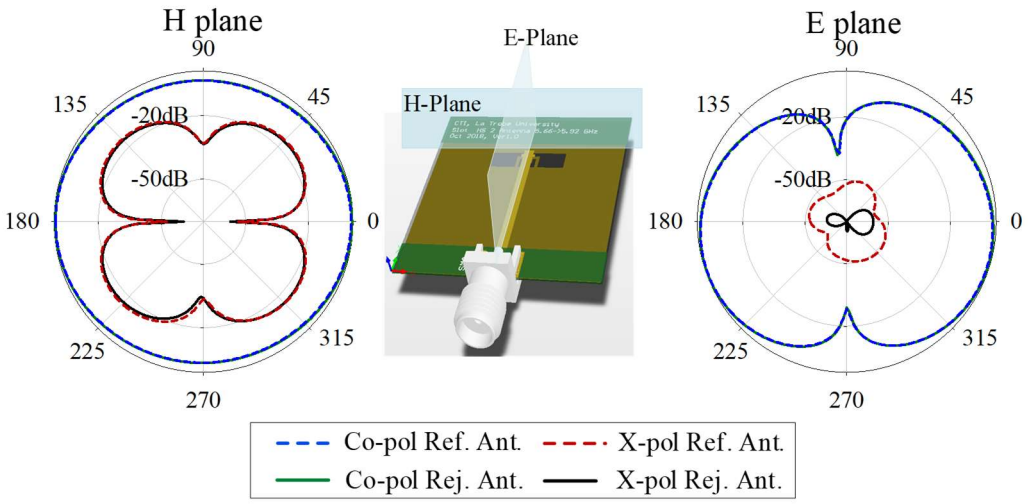


Figure 4-28. Comparison of simulated radiation patterns of the proposed antennas at 5.8 GHz.

second and 16.6 dB at the third harmonic frequencies in the radiation pattern.

Next, the radiation patterns of both antennas at the fundamental frequency are simulated and shown in Figure 4-28. The co-polarization radiation patterns of both antennas at the fundamental frequency are similar to each other and comparable to a simple slot antenna. This means that the added harmonic suppression structures do not alter the gain and radiation pattern at the fundamental frequency.

4.4.3 Summary

In this work, a new small-sized slot antenna with harmonic suppression characteristics over the second and third harmonic frequencies was proposed. The return losses are very high at the second and third harmonic frequencies, 0.53 dB and 0.75 dB, respectively, compared to the conventional slot antenna, 5.4 dB and 8.2 dB, respectively. The simulated gain of the conventional antenna is 0.55, -0.4 and 4.2 dBi, whereas those of the harmonic suppression are 0.1, -21.4 and -20.8 dBi at the fundamental, second and third harmonic frequencies, respectively. Furthermore, the overall size of the harmonic suppression antenna reduces by 25% compared to the conventional antenna. However, the 10-dB return loss bandwidth of the harmonic suppression antenna is 320 MHz (5.5%), while that of the conventional antenna is 580 MHz (10.2%). This means that the bandwidth is reduced by 4.7 % in exchange for harmonic suppression capability and size reduction. The bandwidth still meets the bandwidth specification of 200 MHz of our industrial project for AM modulation. The size of the proposed antenna is 0.27 x 0.065 (wavelength x wavelength) which is very small. The length of this antenna is 25 % smaller than the length of the 0.36 wavelength of the Double Slot HS Antenna. Therefore, the proposed antenna is suitable for small-sized and narrowband applications. The next section proposes a more novel slot antenna with a strong out-of-band rejection characteristic. A much greater size reduction compared with its conventional counterpart antenna is achieved, showing a significant improvement in design technique. The design also achieves a significant improvement in bandwidth compared with its conventional counterpart antenna instead of exchanging bandwidth with the harmonic suppression capability.

4.5 Wideband Triangle Slot Antenna with Out-of-Band Rejection

The two previous proposed narrow slot antennas have a very promising harmonic suppression characteristic. They are very small-sized slot antennas and are suitable for

narrowband applications. Their design processes are simple and less time consuming with clear background theory. Furthermore, they also achieve moderate size reduction, 8.3% and 25%, compared to their conventional counterpart antennas. Their bandwidths are all larger than 200 MHz, which is suitable for our industrial RFID tag project. However, in this section, a more novel antenna is proposed with an out-of-band rejection characteristic, which is needed in applications which need much greater bandwidth. Furthermore, a much bigger size reduction of 60% is achieved with a significant improvement in bandwidth.

A wideband triangle slot antenna with out-of-band rejection using a two-layer standard printed circuit board (PCB) process is proposed in this section. The antenna covers the whole C band (4 GHz - 8 GHz) including the 5.8 GHz ISM and sub 6 GHz band of 5G. First, a right-angled triangle slot antenna is designed as a reference with a centre frequency of 5.8 GHz and a 10-dB return loss bandwidth of 1.17 GHz corresponding to a 20% fractional bandwidth (FBW). Then, a DGS and a thin microstrip line section are integrated into the antenna to achieve out-of-band rejection. This prevents noise and unwanted interference to the receiver and suppresses the high-order harmonics from the transmitter. In addition, the added DGS and thin microstrip line improve the bandwidth to 5.51 GHz (82.7% FBW). The return loss of the proposed antenna is measured up to the third harmonic of the highest working frequency and compared with the reference triangle slot antenna to validate the rejection concept. The out-of-band return loss remains smaller than 1.2 dB by up to 26.5 GHz. The maximum rejection is 33.8 dB at 26.37 GHz compared to the reference triangle antenna. The antenna has a high tolerance against manufacturing errors in relation to both operating and rejection bandwidth, which is validated through deviation investigation. The overall size (including ground) of the antenna is 36 mm x 32 mm, which is small enough to integrate into portable wideband devices using conventional packaging process.

Here, a wideband triangle slot antenna is proposed with a very high out-of-band harmonics and interference rejection, while achieving a compact size and high out-of-band return loss goals. Unlike the previous works, in the design, the DGSs are embedded inside the main radiating slot, avoiding a size increase due to the added suppression components. An analysis of different components of the antenna also shows their effect on return loss. In particular, the rejection mechanism is first illustrated using an analytical equivalent circuit model and is then verified by the simulations and measurement results of a fabricated antenna prototype.

4.5.1 Simple Triangle Slot Antenna

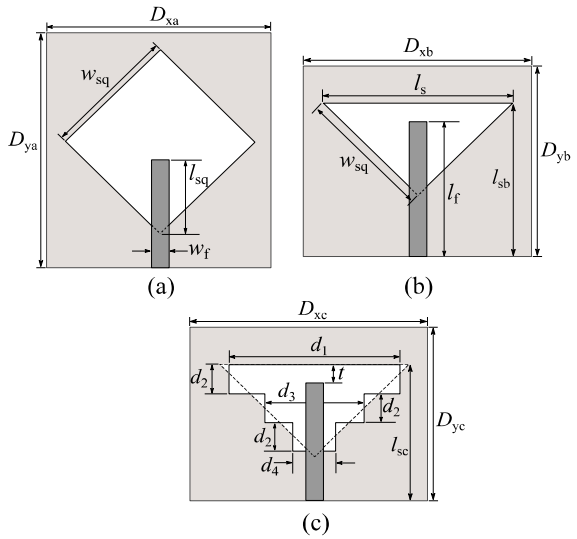


Figure 4-29. (a) Layout of the rotated square slot antenna. (b) Right triangle slot antenna. (c) Three-section tapered slot antenna. The light grey area shows the ground metallization and the dark grey area shows the microstrip metallization. The geometrical dimensions are: D_{xa}= 80 mm, D_{ya} = 80 mm, D_{xb} = D_{xc} = 36 mm, D_{yb} = D_{yc} =32 mm, w_{sq} = 24 mm, w_f= 1.56 mm, l_{sq} = 12.67 mm, l_{sb} = 20.8 mm, l_s =33.94 mm, l_f= 16.8 mm, l_{sb} = 20.8 mm, d_1 = 25 mm, d_2 = 5.7 mm, d_3 = 21 mm, d_4 = 5.4 mm, t = 5.62 mm, l_{sc} = 20.8 mm.

The triangle slot antenna is initially designed based on the rotated square slot antenna shown in Figure 4-29 (a) [103]. The rotation angle is 45°. The side dimensions of the rotated square slot antenna can be roughly determined using the half-wavelength equation (4.4).

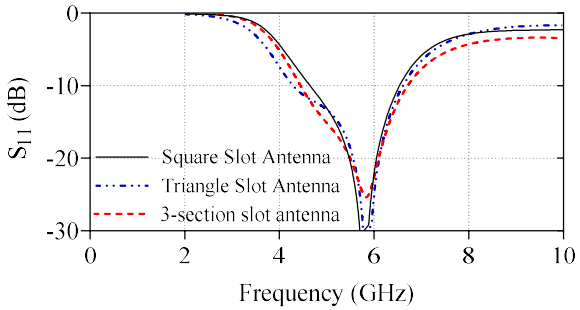


Figure 4-30. Simulated |S11| of rotated square slot antenna, simple triangle slot antenna, and the three-section slot antenna.

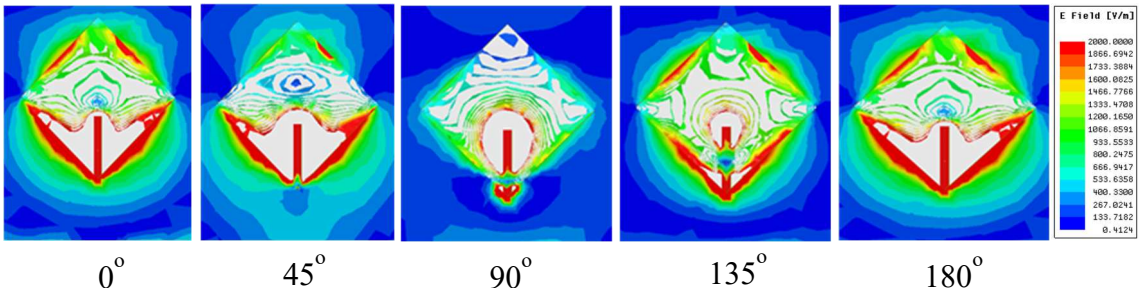


Figure 4-31. Simulated electric field at 5.8 GHz of the rotated square slot. The electric field concentrates mostly on the bottom part.

The optimized value of w_{sq} using the full-wave simulations of the antenna in the Ansoft HFSS is 24 mm which is 2 mm larger than the calculated value of 22 mm (4.4). The feed length l_{sq} in Figure 4-29 is adjusted to achieve a low S_{11} at the center frequency. The simulated S_{11} of the antenna is shown in Figure 4-30. The substrate used in all of the designs and simulations is a 0.508 mm thick Rogers Duroid 5880 with a relative permittivity of ε_r = 2.2 and a loss tangent of 0.0009. The size of the rotated square slot antenna can be reduced by up to 50% by cutting the square slot in half along its horizontal diagonal symmetry line. The working frequency is almost unchanged, as seen in Figure 4-30, when cutting because the electric field is concentrated mainly at the bottom part of the rotated square slot, as seen in Figure 4-31. This figure was generated using the HFSS simulation of the electric field in a half cycle every 45° step. The other half cycle is similar; thus, it is not shown here for brevity.

This creates a right triangle slot antenna shown in Figure 4-29(b). The working principle of the triangle slot antenna can be explained based on the tapered slot principal in [104] [105]. The travelling wave structure in [104] has an open ending which allows the electric field to radiate from it, leading to an endfire radiation pattern. The proposed triangle slot antenna has a closed ending, which turns the antenna into a standing-wave solution and turns the radiation from end fire to broadside. The closed ending also introduces a reactive element into the impedance, thus limiting the bandwidth. As a result, the bandwidth of the triangle slot antenna is limited to only 20%, while the bandwidth of the travelling wave structure is much larger.

The continuous taper of the triangle slot antenna can be modelled by a number of stacked rectangular slot sections of different lengths as shown in the three-section scenario of Figure 4-29(c). As the frequency varies, different rectangular sections resonate resulting in a wide bandwidth. The lowest cut-off frequency is estimated based on the maximum length of the rectangular sections, which is l_s [104]. Using (4.4), $f_{\min} =$ 3.75 GHz for l_s = 33.94 mm. Theoretically, the highest operational frequency is estimated based on the thickness, t, of the substrate as [104]:

$$f_{\max} = 0.03\frac{c}{t(\sqrt{e_r} - 1)} \tag{4.17}$$

This results in f_{max} = 36.6 GHz for h = 0.508 mm. In reality, the higher cut off frequency is mainly determined by the feed matching network, substrate properties and geometry of the antenna. In order to verify the above analysis, the return loss of a three-section staircase slot antenna shown in Figure 4-29(c) is simulated using the Ansoft HFSS and the results

are compared with the simulation results of the triangle slot antenna in Figure 4-29(b). The ground size is the same for the antennas in Figure 4-29 (b) and (c). The designed dimensions are provided in the caption of Figure 4-29. As shown in Figure 4-30, the return loss of both the antenna is similar to each other from 2 to 10 GHz, verifying the above analysis. To sum up, by using a small modification (a simple cutting), the size of the antenna is significantly reduced by up to 50% compared to the rotated square slot antenna.

4.5.2 Wideband and Compact Slot Antenna with Harmonic Suppression

The proposed slot antenna is designed based on the following steps. First, the 90º-corner of the slot is modified to create a triangle DGS (Figure 4-32). The impact of the triangle DGS in out-of-band rejection can be observed by comparing the results in Figure 4-33(a) and (b) (solid black curve). The DGS extends the bandwidth to the left and suppresses the higher-order out-of-band harmonics. It is then further optimized to a rectangular shape shown in Figure 4-32(b) to achieve a smaller slot size and wider bandwidth. The impedance of the microstrip feedline is coupled with the impedance of the rectangular DGS [2], resulting in a high impedance at high frequency. Consistent with this analysis, the stand-alone microstrip coupled rectangular DGS (see inset of Figure 4-32(a)) has a high insertion loss at high frequency (from 10 GHz and above) as seen in Figure 4-32(a).

The initial length, l_d, of the DGS is calculated using the half wavelength equation (4.4). The DGS is designed to suppress the third harmonic of the fundamental 5.8 GHz. So, the resonance frequency of DGS is set to 17.4 GHz. This results in l_d = 7.35 mm. After the simulation-based optimizations to insert the rectangular DGS completely inside the triangle slot for maintaining a compact size, l_d = 6.8 mm is used.

It is clear from Figure 4-33(a) and (b) that the rectangular DGS improves the FBW by exciting another resonance inside the main radiating triangle slot and provides out-of-band rejection up to 26.5 GHz. However, due to the rejection limitation of a DGS, the $|S_{11}|$ of the antenna in Figure 4-32(b) in the rejection region is smaller than -1 dB and has some ripples in most frequencies.

In order to achieve a flat |S11| > -1 dB in the rejection region, a thin microstrip line section is considered in series with the microstrip-line-coupled DGS as shown in Figure 4-32(c). In general, the thin microstrip transmission line is well known as a high-impedance

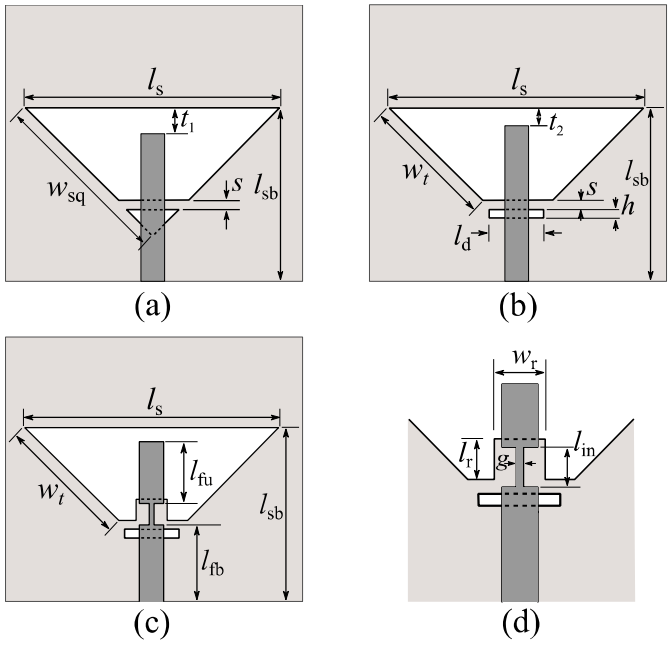


Figure 4-32. Harmonic suppression with (a) a triangle DGS, (b) a rectangular DGS, (c) a rectangular DGS and a thin microstrip section in the feed line. (d) Zoomed view of the microstrip feed line with a narrow section coupled to a rectangular DGS. The light grey area shows the ground metallization and the dark grey area shows the microstrip metallization. The geometrical dimensions are s = 0.6 mm, t_1 = 2.87 mm, w_t = 16.93 mm, h = 0.72 mm, l_d = 6.8 mm, l_{fu} = 9.1 mm, l_{fb} = 8.33 mm, l_r = 2 mm, w_r = 3.6 mm, l_{in} = 1.9 mm, g = 0.2 mm. The ground plane dimensions are the same as the antenna in Fig. 1(b).

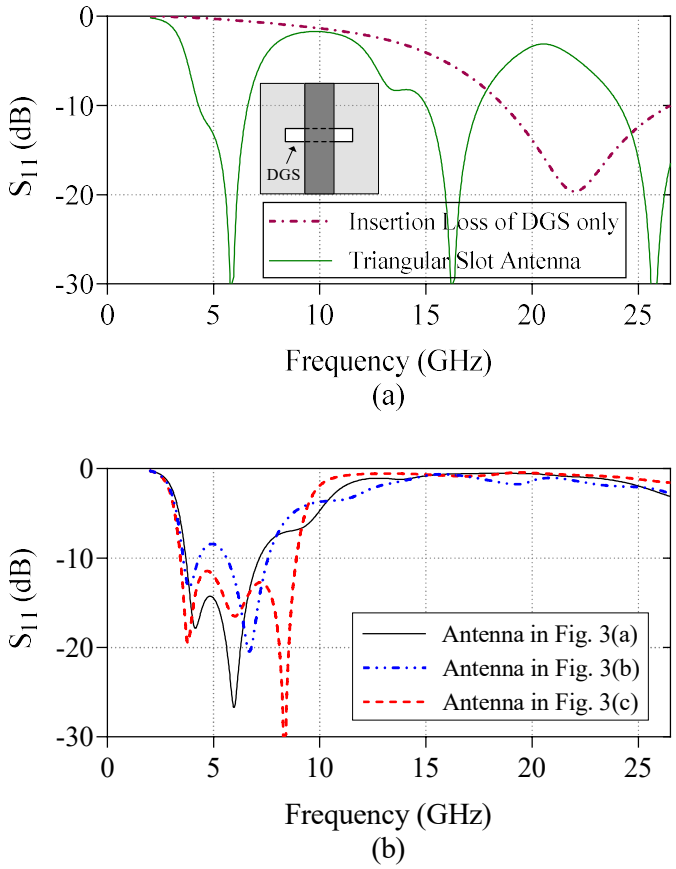


Figure 4-33. (a) $|S_{11}|$ of the reference triangle slot antenna and $|S_{21}|$ of the microstrip loaded DGS shown in the inset. (b) Impact of triangle, rectangular DGSs, and thin microstrip line on the $|S_{11}|$ of the triangle slot antenna.

inductor [50]. However, as shown in Figure 4-33(b), the thin microstrip line acts as an impedance matching circuit more than a filter. It degrades the impedance matching between the microstrip feed line and the slot antenna from 10 GHz and above. In the range of operating frequency, the thin microstrip line helps transform the high impedance of a wide slot line at high frequency (around 8.3 GHz) to 50 Ohm characteristic impedance of the feedline [97]. In addition, the stub below it alters the length and mutual coupling of some stacked rectangular sections (stated in section II) at the shorter portion of the triangle slot. Thus, they together excite another resonance frequency at 8.3 GHz, which is at a higher section of the new operating bandwidth. The position, length and width of the thin microstrip line and the stub are optimized to achieve a 10-dB return loss across the operating bandwidth while maintaining the flat |S11| > 1 dB in the rejection region.

As seen, the reflection coefficient of the slot antenna of Figure 4-32(c) shows a high bump at 5 GHz (Figure 4-33(b)), which might elevate to above -10 dB in the fabrication prototype due to inevitable manufacturing tolerance. Therefore, the return loss at this frequency should be optimized to be as low as possible. This is achieved by altering the mutual coupling and length of the stacked rectangular sections (stated in section II) at the longer portion of the triangle slot. The final design is obtained by adding two right-triangular sections to the sides of the main radiating slot (shown in the inset of Figure 4-34). In addition, the two top sides of the main radiating slot are truncated to a 90° angle. It is clear from Figure 4-34 that these elements improve the return loss at the lower section of the operating bandwidth, from 3.5 GHz to 6.5 GHz, without affecting the rejection region. Furthermore, adding these elements also reduces the ground size by 11%, which can be seen in Figure 4-36.

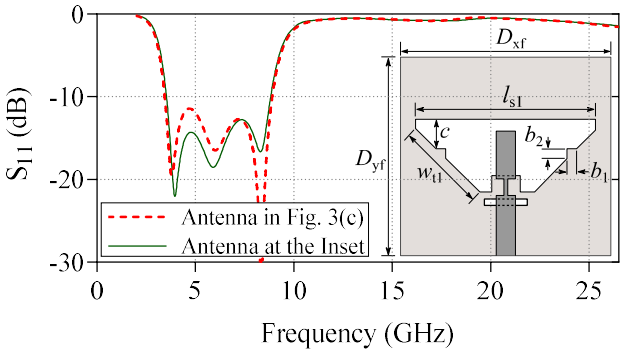


Figure 4-34. A comparison between the simulated $|S_{11}|$ antenna in Figure 4-32(c), and the final optimized antenna shown in the inset. The dimensions are s =0.6 mm, l_{sl} =28 mm, c =6.47 mm, w_{tl} =9 mm, $b_1 = b_2$ =2.06 mm, D_{xf} = 32 mm, D_{yf} =32 mm. All the other dimensions are the same as in Figure 4-32 (c).

Finally, Figure 4-35 shows the simulated return loss of the final design with the deviation of 0.4 mm from the top layer to the bottom layer, that is, the deviation of the feed line with the slot antenna in vertical and horizontal directions.

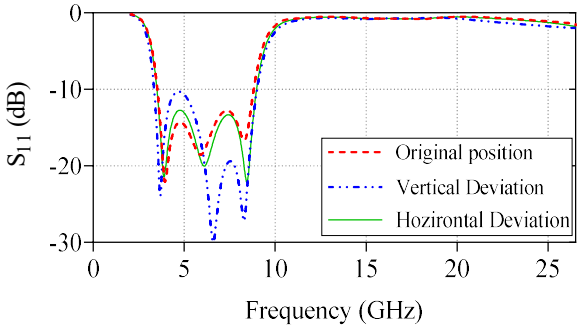


Figure 4-35. Dimensional tolerance impact with 0.4 mm offset of the top and bottom layer in the final optimized antenna.

The return loss is better than 10 dB in operation frequency in all cases. This means the final design can tolerate up to 0.4 mm deviation in both directions. The results also confirm the necessity to further optimize the performance at 5 GHz.

Figure 4-36. Photograph of the fabricated antennas. The proposed antenna is on the left side of each photo, whereas the simple triangle slot antenna is on the right.

4.5.3 Results and Discussions

The front and back views of both the fabricated prototypes are presented in Figure 4-36. The measured return losses of the fabricated antennas using the Anritsu MS4644B network analyser are shown in Figure 4-37 together with the full-wave simulation results. The working frequency range of the reference triangular slot antenna is 5.23 - 6.41 GHz, showing a 10-dB FBW of 20%. The designed compact antenna operates between 3.65 - 8.75 GHz at 10-dB return loss, showing an FBW of 82.2%.

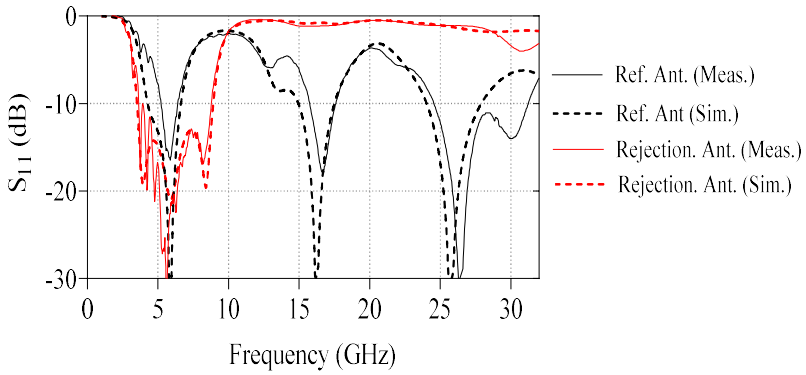


Figure 4-37. The simulated and measured reflection coefficient of the reference and the proposed antennas.

It also achieves a wide out-of-band rejection from 11 GHz up to 29.8 GHz, corresponding to 3.38f_h, where f_h is the highest working frequency of the antenna. The maximum rejection is 33.8 dB at 26.37 GHz compared to the simple triangle antenna. The $|S_{11}|$ remains higher than -1.2 dB up to 26.5 GHz. The radiation patterns of both the reference triangle-slot antenna and the proposed antenna are measured in an anechoic chamber setup. Measurements are performed at 5.8 GHz for both antennas, and at 3.65 and 8.81 GHz for the rejection antenna only (Figure 4-39). The two antennas show a very similar radiation pattern at 5.8 GHz.

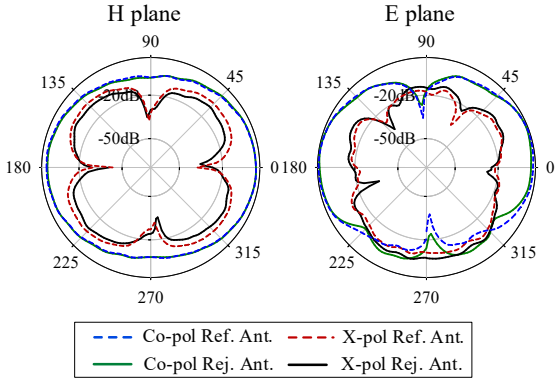


Figure 4-38. The measured radiation pattern of the reference and the proposed antennas at 5.8 GHz.

The gain of the simple triangle antenna at 5.8 GHz is 5.3 dBi, whereas the proposed antenna gain is 5.25 dBi at 5.8 GHz. This verifies that the added parts for harmonic rejection have a minimal effect on the gain of the antenna at 5.8 GHz. The measured gain in boresight is plotted versus frequency in Figure 4-40. The antenna shows a maximum gain of 5.8 dBi at 6.4 GHz.

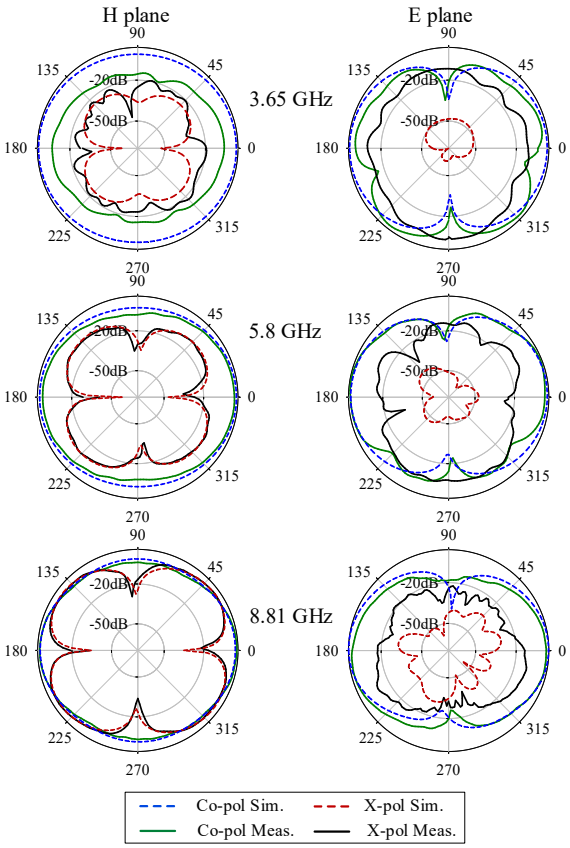


Figure 4-39. Simulated and measured radiation patterns of the rejection antenna.

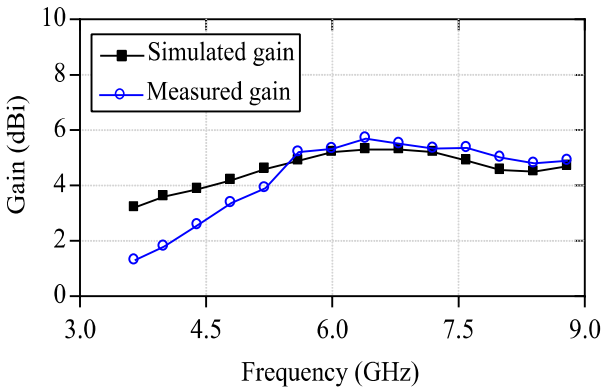


Figure 4-40. Measured and simulated gains of the proposed antenna.

4.5.4 Comparison with Other Designs

Table 4-3 compares the designed antenna and the state-of-art designs in terms of various performance metrics. Based on the table, it can be seen that the proposed antenna has the widest FBW and largest realized gain among the others. The antenna shows a wide rejection bandwidth of 1.15 f_h – 3.38 f_h, where f_h is the highest working frequency of the antenna. This corresponds to 19.6 GHz absolute rejection bandwidth. The $|S_{11}|$ within the

rejection band remains larger than -1.2 dB up to 26.5 GHz showing the highest out-of-band rejection with respect to the previously designed antennas. Another important metric in the harmonic suppressed antennas is the antenna size change and the overall size or the ground size of each antenna. According to the table, the proposed antenna offers 60% size reduction in the main radiating slot, compared with the rotated square slot antenna. From Table 4-3, it can be seen that the proposed antenna has the second-smallest ground size, calculated in one wavelength unit (double the value in equation (4.4)) based on the lowest operating frequency. Overall, the designed antenna shows a highly competitive performance in comparison with the state-of-the-art harmonic suppressed antennas in the literature. The wide bandwidth of the antenna is achieved due to a proper combination of the triangle slot shape and matching circuits, while the small size is because of the matching elements and the simple cut (see section 4.5.1 and 4.5.2). Furthermore, the small width of ground that surrounds the slot reduces the overall size of the antenna. The gain at higher frequencies is around 5 dBi while the gain at lower frequencies is about 2-3dBi, which is reasonable compared to the other narrow band designs shown in Table 4-3.

4.5.5 Summary

An out-of-band rejection triangle-slot antenna has been demonstrated to have highly competitive performance. The miniaturization of ground size is achieved by a simple cut and adding matching elements. The fabricated prototype shows a high potential for suppressing unwanted harmonics and interference in wireless communication systems. The highly compact size of the antenna makes it suitable to be integrated into portable wideband devices. Compared to the two previous narrow slot antennas, the proposed antenna shows a significant improvement in terms of size reduction, compared to reference antennas. Furthermore, the bandwidth is increased significantly with added harmonic suppression structures, which is opposite to the two previous narrow slot antennas where their bandwidths are reduced.

4.6 Summary

In this chapter, by applying the DGS technique together with the SIR structure, fringing capacitor, and thin microstrip line techniques, harmonic suppression is achieved with a very strong rejection capability, 1 to 2 dB of return loss at the rejection region without affecting the gain at a fundamental frequency. Furthermore, a size reduction is obtained in all three designs, 8.4% for the Double Slot Harmonic Suppression Antenna, 25% for the Small Size Slot Harmonic Suppression Antenna, and 60% for the Wideband Triangle Slot Antenna

with Out-Of-Band Rejection compared with their conventional counterpart antennas. In addition, in the wideband antenna, the insertion of the harmonic suppression structure also helps widen the bandwidth to 83% from 20%. All of the three antennas fulfil the goals of miniaturization, longer battery lifetime, and lower cost. The three harmonic suppression antennas cover both narrow band and very wide band applications. Furthermore, because of their small size, they are suitable for portable RF devices.

Table 4-3. Performance Comparison.

Ref.	**Rejection Techniques**	**Centre freq. (GHz), -10 dB FBW**	**Max. Gain (dBi)**	**S_{11} > -3 dB**	**Min. S_{11} in rejection band (dB)**	**Ant. Size change (%)**	**Ground size (wavelength)**
[54]	MIM cap and narrow microstrip line	3.5, 57%	4.56	$1.1 f_h$ - $3.33 f_h$	-2	0	0.9 x 0.82
[55]	Narrow gaps and thin line	5.55, 18%	3	f_h - $3f_h$	<1	N/A	0.68 x 0.44
[56]	Photonic bandgaps	2.25, 70%	4.6	$1.1 f_h$ - $1.67 f_h$	-1.5	> +22	N/A
[57]	DGS	2.49, 8.4%	3.27	$1.15 f_h$ - $3.34 f_h$	-3.8	7.6	0.61 x 0.51
[58]	Coupling slot filters	2.4, 8.7%	3.9	N/A	-7.5	-3	1.1 x 0.9
[59]	Two folded L-shaped slots	2.4, 9.5%	0.92	$1.25 f_h$ - $1.87 f_h$	-5	0	0.38 x 0.24
[60]	Stepped-Impedance slot	4.5, 8.8%	4	$1.06 f_h$ - $2.34 f_h$	-7	-32	N/A
[61]	Wiggly-line band-stop filter	2.37, 3.8%	5	$1.1 f_h$ - $3.3 f_h$	-2	N/A	0.57 x 0.38
[106]	Bottom transverse slot	2.5, 13.9%	3.6	$1.34 f_h$ - $2.3 f_h$	-8	-42	0.52 x 0.52
[107]	Folded thin strips	2.5, 1.44%	3.6	$1.1 f_h$ – $7.2 f_h$	-2.5	-88.9	0.78 x 0.54
T. W.	**DGS and narrow microstrip line**	**6.23, 83%**	**5.8**	**$1.15 f_h$ - $3.38 f_h$**	**-1.2**	**-60**	**0.46 x 0.46**

Chapter 3 described the successful development of a Power Amplifier (PA) with the PMOS linearity technique to increase P_{1dB}, which can achieve a high PAPR, and thus the high data rate goal. The PA achieves competitive performance with the lowest DC quiescent current, small chip size and moderate P_{1dB} at the highest frequency and the lowest supply voltage, compared to the state-of-the-art PAs in the literature. Furthermore, the proposed PA has noise immunity due to its differential structure, which is not available in the single-ended structure. With this improvement in P_{1dB}, the PA meets the demand of high linearity in modern wireless communications with higher peak-to-average power ratio (PAPR) standards. The high PAPR allows a large number of independently modulated subcarriers, thus leading to a high data rate transmission.

However, for future applications, there is a higher demand for spectral resources due to the huge increase in bandwidth and the number of wireless devices. Although the data rate enhancement, and thus spectral resources, which is achieved by improving the linearity of PAs and suppressing high-order harmonics using antennas, is significant, there are other ways to address this demand. In-band full-duplex (IBFD) systems, in which wireless terminals are allowed to transmit and receive in the same frequency band, have recently gained attention.

The IBFD operation is of great interest in compact communication systems due to their capability to double spectral efficiency, hence improving the data rate. However, the IBFD is still not widely used due to self-interference, in which radio signals from its own transmitter (TX) can be received by the receiver (RX). Due to passiveness, hence, simplicity, antenna isolation techniques are in high demand. They can also help to reduce the complexity of self-interference cancelation in the digital domain. Therefore, research on high isolation antennas is necessary and can be used to drive future research and accelerate the inclusion of IBFD technology within an upcoming wireless standard.

The next chapter proposes a full-duplex antenna working at 5.8 GHz ISM band and describes its design process. The proposed full-duplex antenna achieves a very high isolation, about 50 dB, across its operating bandwidth. The bandwidth of the proposed antenna should be more than the average of the recent IBFD antenna designs. The novel isolation technique is proposed without the use of a coupler to achieve device compactness. To target a low-cost fabrication, like the three harmonic suppression antennas, the full-duplex antenna is designed with a single-layered substrate.

5 Full-Duplex Antenna

In the two previous chapters, the PA meets the demand of high linearity in modern wireless communications with higher peak-to-average power ratio (PAPR) standards, leading to high data rate transmission, while three harmonic suppression antennas achieve the goals of miniaturization, longer battery lifetime, and lower cost. Moreover, each design achieves one or two more sub-goals including low quiescent current in the CMOS PA, and wide bandwidth in the triangle slot antenna. These performance improvements can help RF transceivers become more competitive in terms of compactness, high data rate, strong interference immunity, and longer battery life.

However, for future applications, there is a higher demand for spectral resources due to the huge increase in bandwidth and the number of wireless devices. Although the data rate enhancement, and thus spectral resources, which is achieving by improving the linearity of PAs and suppressing high-order harmonics using antennas, is significant, there are other ways to address this demand. The in-band full-duplex (IBFD) operation is of great interest in compact communication systems due to the capability of doubling the spectral efficiency, hence improving the data rate. Due to passiveness, hence, simplicity, antenna isolation techniques are in high demand. They can also help to reduce the complexity of self-interference cancelation in the digital domain. Therefore, research on high isolation antennas is necessary and can be used to drive future research and accelerate the inclusion of IBFD technology within an upcoming wireless standard.

This chapter develops a compact and a low-profile antenna with a very high isolation of 50 dB for full-duplex systems while maintaining an average 10 dB impedance bandwidth, achieving the aims of low cost and small size. This can be done by overcoming a 30-dB limitation in isolation of orthogonal polarizations in a single antenna using an additional isolation improvement technique.

A single-layered slot antenna system working at a 5.8 GHz ISM band is proposed for IBFD applications without the use of a coupler to achieve a small size. First, high isolation is achieved by the strong separation of even-mode and odd-mode feeds. The microstrip-coupled coplanar waveguide (CPW) is used at Port 1 (TX port) to excite a stepped-slot antenna in the CPW odd mode. On the opposite side, a microstrip T-junction power divider is employed at Port 2 (RX port) to feed two offset-fed stepped-slot antennas in even mode. Second, isolation is further improved by 30 dB by using a lumped capacitor at the

termination of the CPW. The measured isolation between the two ports is more than 50 dB across the bandwidth. The measured -10 dB bandwidth of Port 1 is 0.49 GHz (8.5%) while that of Port 2 is 1.06 GHz (18.3%). The gains of TX and RX antennas are 5.4 dBi and 5.8 dBi at 5.8 GHz. The proposed antenna can also be deployed as a dual-polarized antenna. Mathematical analysis and equivalent transmission line circuit models are provided to give physical insight into the working principles of the antenna with validation from the ANSYS HFSS simulation.

5.1 Introduction

The IBFD is of great interest in compact communication systems due to the capability of doubling the spectra efficiency [27]. An IBFD system allows transmitting and receiving on the same frequency simultaneously. However, IBFD systems are still not widely used due to self-interference, in which radio signals from its own transmitter (TX) can be received by the receiver (RX). In fact, the power of a self-interference (SI) signal can be a million times higher than the power of the received signal. Therefore, several techniques have been proposed to improve the isolation between collocated TX and RX. Due to passiveness, hence, simplicity, antenna isolation techniques are in high demand. They can also help reduce the complexity of self-interference cancelation in the digital domain.

There are several antenna isolation techniques such as orthogonal polarization [66, 67], even-mode and odd-mode excitation in CPW [41, 68], differential feeding [29, 69, 70], coupler [42-44], and parasitic /decoupling resonating structures [45, 71]. The orthogonal polarization method using the two separated radiating elements in [66, 67] can achieve around 25 dB isolation. However, the two radiating elements occupy a large space, which is not suitable for the need for miniaturization. Another method [41, 68], using a single radiating element and thus a smaller space, utilizes the even mode and odd mode in CPW to achieve high isolation between the two ports (leading to ~ 20 to 30 dB isolation).

The differential feeding method in [69] uses the geometrical symmetry of the two spiral antennas to cancel the coupled TX voltage at the RX port, achieving an isolation of about 40 to 50 dB across a wide bandwidth. However, it requires a complex and costly 3D design. The method in [29, 70] also uses the differential feeding method but for rectangular patch antennas. The isolation is improved further, up to 90 dB, by using additional 3dB/180^{o} ring hybrid couplers. However, this isolation value can only be achieved in a very limited bandwidth. Additionally, the feeding network including couplers occupies a critically large area. Couplers are also used in [42-44] to improve isolation by up to 35 dB. Those couplers form a differential structure using a half wavelength delay line between their two ports,

leading to opposite phases. Nevertheless, the size of these couplers is usually large, or the number of fabricated layers must increase. The decoupling structures in [45, 71], which are basically resonators, increase the isolation up to 50 dB. This method uses two separated radiating elements plus resonators, thus significantly increasing the size. The antenna in [46] uses the reflective termination method. However, it has two separated antennas with two layers, leading to a size and cost increase.

In this chapter, a slot antenna system with very high isolation is proposed without the use of a coupler to achieve device compactness. First, the even mode and odd mode method in a CPW is used to obtain moderate isolation with a single radiating element and thus a smaller space. Second, a capacitor is used at the termination of the CPW to further improve the isolation by terminating the reflection coefficient without changing the size.

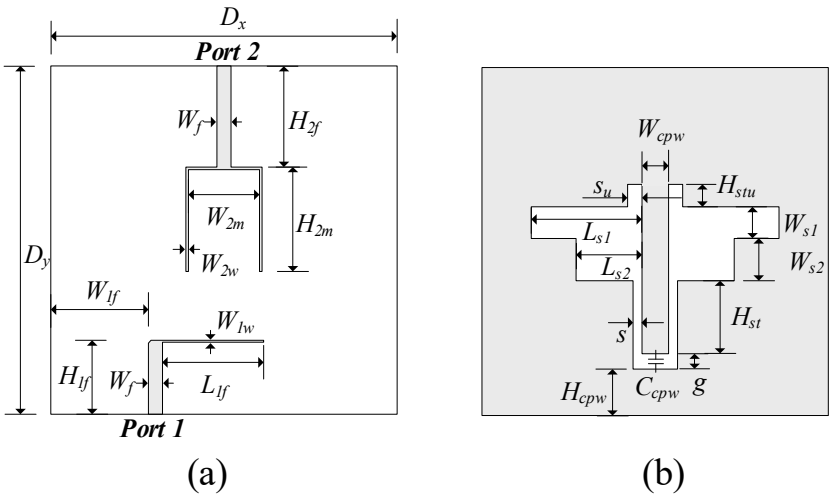


Figure 5-1. (a) Top layer. (b) Bottom layer. The geometrical dimensions are: D_x = 45 mm, D_y= 40 mm, W_f= 1.56 mm, H_{2f}= 11.2 mm, H_{2m}= 11.6 mm, W_{2m}= 8 mm, W_{2w}= 0.3 mm, W_{1w}= 0.2 mm, W_{1f} =15.04, L_{1f}= 11.4 mm, H_{1f}= 8.2 mm, W_{cpw}= 1.4 mm, s_u= 0.58 mm, H_{stu}= 2.5 mm, W_{s1}= 3.5 mm, L_{s1}= 13.25 mm, W_{s2}= 4.7 mm, L_{s2}= 8.2 mm, H_{st}= 9 mm, s= 0.2 mm, g= 0.8 mm, H_{cpw}= 6.5 mm, C_{cpw}=0.65 pF.

5.2 Antenna Design

5.2.1 Analysis of Even and Odd Mode in CPW

The proposed antenna is described in Figure 5-1 with the geometrical dimensions. The substrate used in the fabricated design and simulation setting is a 0.508 mm-thick Taconic TLY-5 with a relative permittivity (ε_r) of 2.2 and a loss tangent of 0.0009. As can be seen in Figure 5-1, at Port 1, a microstrip feeding line is coupled with a CPW-slotline tee to have the antenna operated in odd mode only. Port 2 uses a T- junction power divider to form a conventional array slot antenna working in even mode only.

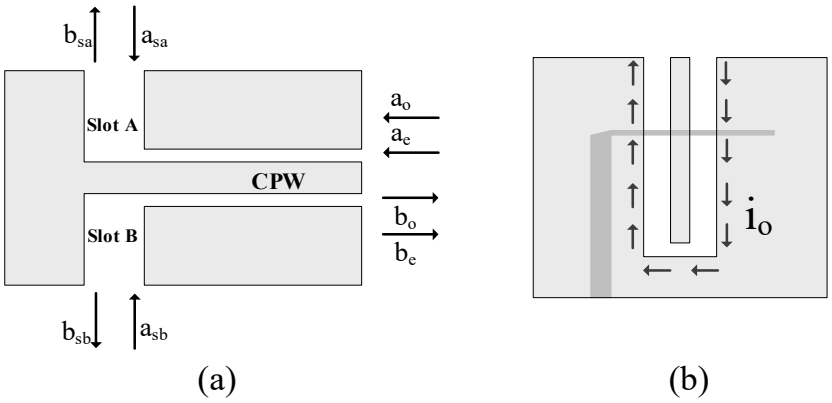


Figure 5-2. (a) CPW-slotline tee. (b) Microstrip coupled CPW with the surface current I_o in odd mode.

Figure 5-2 (a) shows a CPW-slotline tee which is used frequently in uniplanar hybrid structures. The incident and reflected waves at the transition plane are a_e, a_o, a_{sa}, a_{sb}, and b_e, b_o, b_{sa}, b_{sb}, respectively. The relationship between incident and reflected waves of the CPW-slotline tee is [108]:

$$\begin{bmatrix} b_e \\ b_o \\ b_{sa} \\ b_{sb} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} -1 & 0 & 2 & 2 \\ 0 & 1 & -2 & 2 \\ 2 & -2 & 0 & 1 \\ 2 & 2 & 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} a_e \\ a_o \\ a_{sa} \\ a_{sb} \end{bmatrix} \tag{5.1}$$

From (5.1), if $a_{sa} = a_{sb}$ or the slot A and B are excited symmetrically and when a_o =0, only even mode in coplanar is generated as b_o =0. In addition, if the CPW is excited in odd mode only and no excitation is fed to slot A and B, or $a_e = a_{sa} = a_{sb} = 0$, then $b_{sa} = -b_{sb}$ or the CPW-slotline tee will propagate differential waves out of slot A and slot B. Therefore, a CPW-slotline tee can be excited to propagate even mode and odd mode waves.

In order to excite the CPW-slotline tee in odd mode, a microstrip line-coupled CPW structure, as seen in Figure 5-2(b), is used [41, 68].

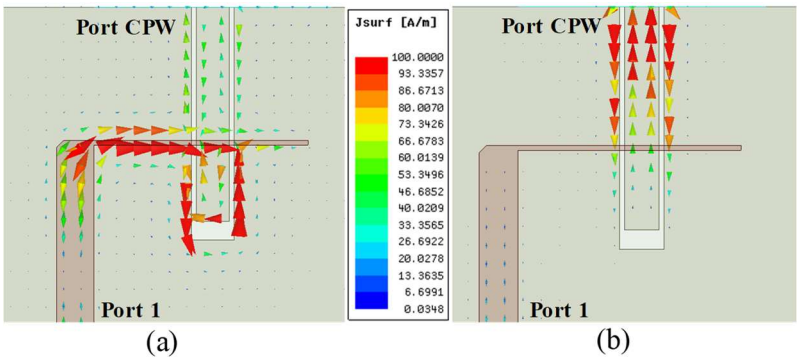


Figure 5-3. Surface current vector in CPW coupled microstrip. (a) HFSS simulation at 5.8 GHz of surface current vector in odd mode. (b) HFSS simulation at 5.8 GHz of surface current vector in even mode.

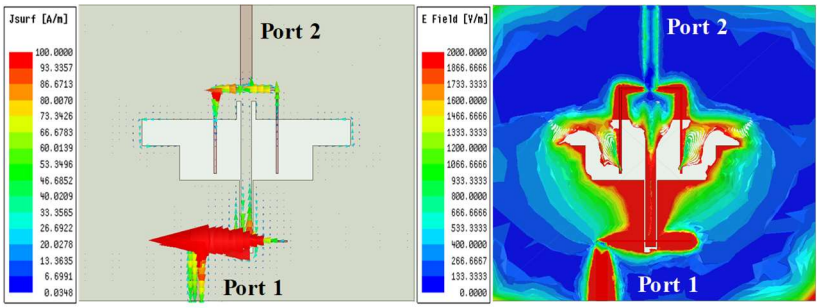
The simulated surface current in Figure 5-3(a) shows that when the transverse microstrip line is excited, the coupled surface current flows in opposite ways along two

sides of the CPW, which is the odd mode current. However, when the CPW is fed by the even mode signal, there is almost no signal coupled from the two slotlines of the CPW to the transverse microstrip line, as seen in Figure 5-3(b).

5.2.2 Isolation Investigation

This section discusses the isolation between the two feedings.

As seen in Figure 5-1, when Port 1 is excited, the signal generated from the transverse microstrip line will be fed to a one-wavelength-CPW fed-inductive slot antenna [109]. This signal is coupled to the CPW in odd mode, flowing to the two stepped slots differentially through the CPW-slotline tee (as explained in section II that $b_{sa} = -b_{sb}$). Then, these two differential signals, which are coupled to the two thin microstrip lines at the two ports of the T-junction power divider, will cancel each other out and will not appear at its output port (Port 2) of the proposed antenna.

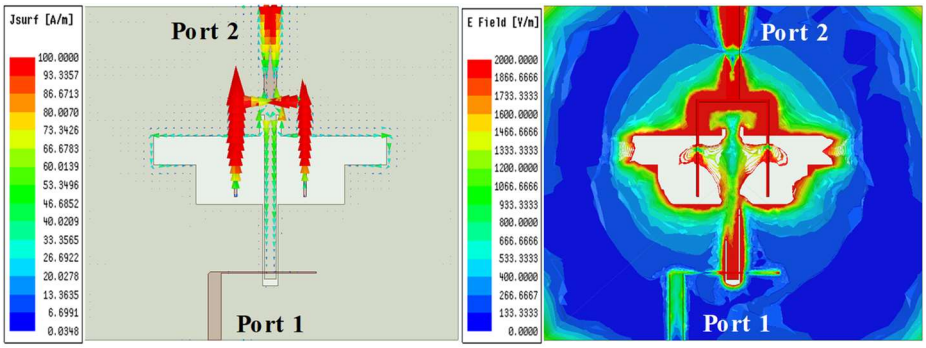


(a) (b)

Figure 5-4. HFSS simulation at 5 GHz of (a) zoomed view of the surface current vector and, (b) electric field magnitude when Port 1 is excited.

It is clear from Figure 5-4(a) that the surface current vectors are opposite at the ports of the T-junction power divider, thus the sum of the surface current is equal to zero at Port 2 of the antenna. However, there is still parasitic signal leaking out to Port 2 due to asymmetricity. Similarly, Figure 5-4(b) shows that there is only a small portion of electric field leaking to Port 2 when Port 1 is excited.

When Port 2 is excited, the signal is divided symmetrically by the microstrip T junction power divider. These two signals are fed to an array of two stepped slot antennas etched in the ground and flow to the CPW-slotline tee only in even mode (as explained in section II when $a_{sa} = a_{sb}$). Because the CPW-coupled microstrip line supports the odd mode signal only, there is no signal flowing to Port 1 except for the parasitic signal due to asymmetricity.



(a) (b)

Figure 5-5. HFSS simulation of (a) surface current vector and, (b) electric field magnitude when Port 2 is excited.

Figure 5-5 shows the HFSS simulation of the surface current vector and the electric field magnitude when Port 2 is excited. As confirmed, there is only a small surface current and electric field leaking to the Port 1.

In practice, the 30-dB isolation of the even and odd mode is far away from the requirement of the full-duplex system. To significantly enhance isolation while keeping the design compact, a capacitor is placed at the end of the CPW, as shown Figure 5-1(b), to cancel out the leaking signals. The working principle of C_{cpw} can be explained using the three-port method in [72]. The third port (Port 3) is at the termination of the CPW where C_{cpw} is placed, as seen in Figure 5-1(b). The coupling coefficient C_{21} from Port 1 to Port 2 can be expressed as

$$C_{21} = S_{21} + \frac{S_{23}S_{31}\Gamma_{\mathrm{L}}}{1 - S_{33}\Gamma_{\mathrm{L}}} \tag{5.2}$$

where S_{21}, S_{31}, S_{23}, and S_{33} are the S-parameters of the three-port antenna structure without a reflective terminal. Γ_L is the reflection coefficient of Port 3.

The coupling S_{21} between Port 1 and Port 2 can be cancelled out by optimizing reflection coefficient Γ_L of the Port 3 using a proper reflective impedance. However, based on equivalent circuits (which are discussed in the next section), this impedance will be loaded into the even mode impedance, thus simultaneously changing S_{21}, S_{23}, and S_{22}. Therefore, several optimization routines are performed to obtain a proper value of Γ_L such that a high isolation and a good matching are achieved simultaneously at Port 2.

To implement Γ_L, it should be noted that it is a complex quantity. However, the real part (implemented by a resistor) should not be implemented because part of the energy from Port 2 will be dissipated on this resistor as heat, thus reducing radiation efficiency or gain of the antenna in even mode. Therefore, only the imaginary part is implemented. Here, a

capacitor is chosen instead of an inductor because of the lower price and smaller steps in commercially available values.

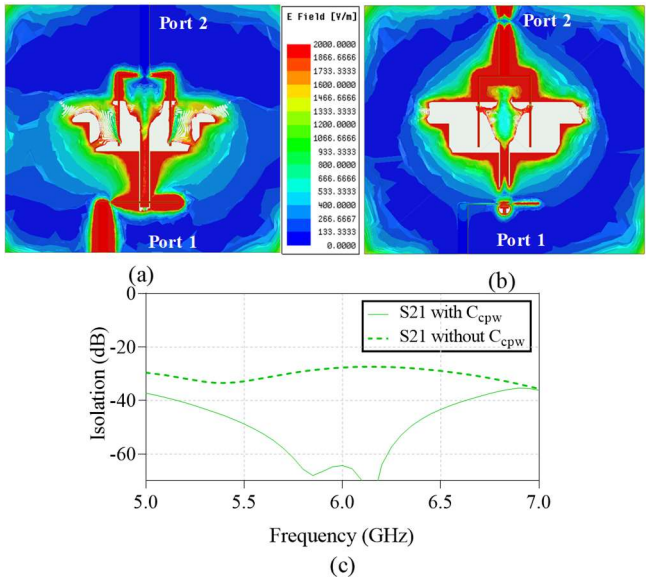


Figure 5-6. HFSS simulation of electric field magnitude with C_{cpw} when (a) Port 1 is excited, (b) Port 2 is excited, (c) Isolation in dB between the two ports.

Figure 5-6(a) and (b) show the HFSS simulation of the electric field magnitude of both Port 1 and Port 2 with C_{cpw}. It can be seen that there is no leaking signal at any port when the other port is excited. Figure 5-6(c) compares simulated isolation in dB between two ports with and without C_{cpw}. It can be seen that C_{cpw} improves isolation by more than 30 dB, from 30 to more than 60 dB in the HFSS simulation.

5.2.3 Antenna Impedance Investigation

This section provides two equivalent transmission line circuit models in the odd mode (shown in Figure 5-7) and even mode (shown in Figure 5-8), thus showing a deeper theoretical insight into the design. It helps to understand the behaviour of S-parameters, when a dimensional parameter changes. It also assists the optimization process since the proposed antenna is a complicated system with two ports and several parameters. Some parameters affect the impedance of one port only while others affect the impedance of both the ports. Furthermore, the isolation is varied during the impedance optimization process due to (5.2).

The stepped slot antenna is etched in the ground plane as shown in Figure 5-1(b). The stepped shape of the slot antenna is chosen in order to reduce the discontinuities from the CPW to the slot antenna, thus having a larger bandwidth. The CPW feeding is employed to match the impedance of the stepped slot antenna to the two ports. An upper CPW-like stub

is created to add more degrees of freedom in optimizing the isolation reduction since it can be used as another port to optimize cancellative reflection, in addition to C_{cpw}.

Port 1 will excite the CPW-fed-inductive stepped-slot antenna coupled with the two microstrip lines H_{2m}. The C_{cpw} has a minimal effect on the impedance of Port 1 because the odd mode electric field along the two slotlines of the CPW will cancel each other at the exact location of C_{cpw}, thus bypassing C_{cpw}.

Figure 5-7 shows the equivalent circuit of the proposed antenna excited from Port 1 using the analysis method in [110]. Figure 5-7(a) describes the antenna with a voltage source V_0, which represents the coupling from the transverse thin microstrip L_{1f} of Port 1 to the CPW. $Z_{sl\text{-}ant\text{-}1}$ is the impedance looking into the slot antenna loaded microstrip lines.

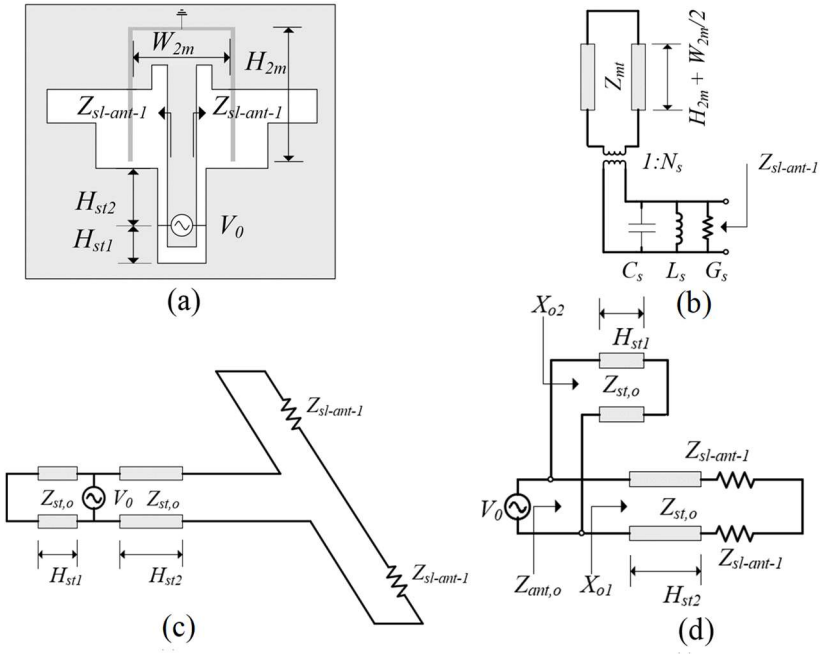


Figure 5-7. (a) Slot antenna excited from the CPW in odd mode. (b) Impedance of the slot antenna loaded microstrip line. (c) Equivalent circuit of the proposed antenna when excited from Port 1. (d) Reduced circuit model of the slot antenna.

Figure 5-7(b) is a simplified equivalent circuit of the microstrip offset-fed slot antenna [111] without any parasitic capacitors. Z_{mt} is the characteristic impedance of the thin microstrip lines H_{2m}. These two thin microstrip lines are terminated to a virtual ground, where two differential signals from Port 1 cancel each other. The coupling section of the thin microstrip line H_{2m} and the slot antenna is represented by an ideal transformer $1{:}\ N_s$. The admittance of one branch of the stepped slot antenna is represented by $1/Z_{sl\text{-}ant} = G_s + 1/j\omega L_s + j\omega C_s$. Figure 5-7(c) is the equivalent circuit of the slot antenna loaded microstrip lines in the presence of the CPW. Here, $Z_{st,o}$ is the characteristic odd mode impedance of the CPW. Figure 5-7(d) is the reduced circuit model of Figure 5-7(c).

The T junction power divider, shown in Figure 5-1(a), is used at Port 2 to feed two stepped slot antennas. Here, there are two offset fed slot antennas [111] coupled with the CPW as shown in Figure 5-1(b). The capacitor C_{cpw} can be utilized to optimize the impedance of Port 2. The reason is that in the even mode, the electric fields that flow along the two slotlines of the CPW will be double at the position of C_{cpw} because they have the same direction. From Figure 5-7, the stepped slot dimensions, the H_{2m}, the H_{st1} and H_{st2} of the CPW affect the impedance, and thus the resonant frequency of Port 1.

The odd mode impedance $Z_{ant,o}$ of the stepped slot antenna coupled microstrip lines is then transformed to 50 Ω impedance of Port 1 using the quarter-wave impedance transformer L_{1f} (in Figure 5-1(a)).

The T-junction power divider, shown in Figure 5-1(a), is used at Port 2 to feed two stepped slot antennas. Here, there are two offset fed slot antennas [111] coupled with the CPW as shown in Fig. 1(b). The capacitor C_{cpw} can be utilized to optimize the impedance of Port 2. The reason for this is that in the even mode, the electric fields that flow along the two slotlines of the CPW will be double at the position of C_{cpw} because they have the same direction.

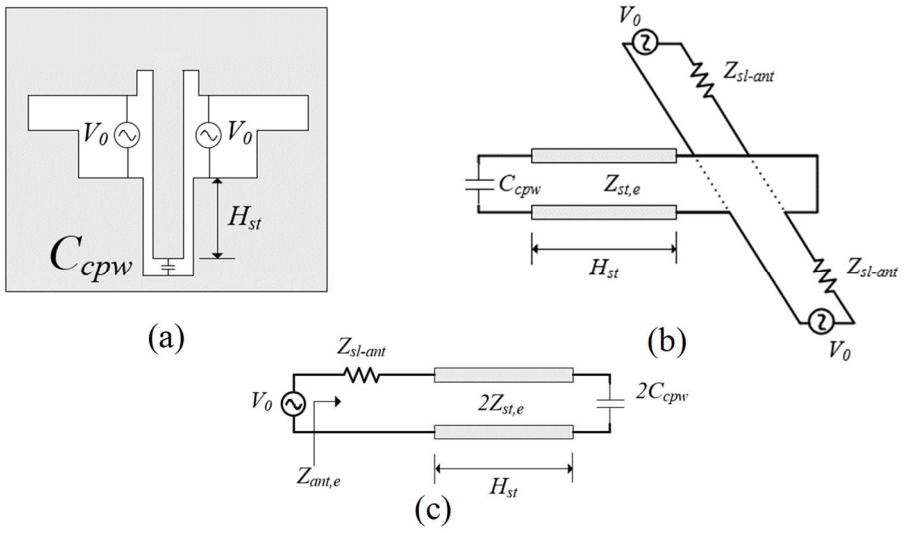


Figure 5-8. (a) Slot antenna excited from the two thin microstrip lines in even mode in the presence of the CPW. (b) Equivalent circuit model in even mode. (c) Reduced circuit model of one slot branch.

Figure 5-8 shows the equivalent circuit model of the offset fed slot antenna fed by two narrow microstrip lines H_{2m} of the T junction power divider when Port 2 is excited. This model is used to investigate the even mode impedance of the offset fed slot antenna in the presence of the CPW. Here, $Z_{st,e}$ is the characteristic even mode impedance of the CPW and $\beta_{st,e}$ is the even mode propagation constant of the CPW, respectively. From Fig. 8,

the stepped slot dimensions, the CPW dimensions, and the C_{cpw} affect the impedance and thus the resonant frequency of Port 2.

The even mode impedance $Z_{\text{ant,e}}$ of the slot antenna is then transformed to 50 Ω impedance of Port 2 through the two ports of the T-junction power divider using the quarter-wave impedance transformer H_{2m} as described in [111].

5.2.4 Parameter Study

This section provides the HFSS simulation results with some of the most sensitive dimensional parameters to assist the design process and validate the proposed equivalent circuit models in the previous section (section 5.2.3).

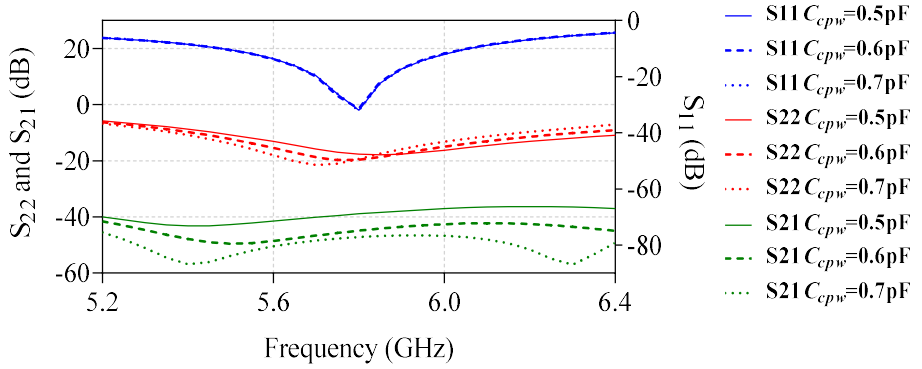


Figure 5-9. Simulated S-parameters with different values of C_{cpw}.

Figure 5-9 shows the S-parameters of the proposed antenna with different values of C_{cpw}. It is clear that S_{11} does not vary while the resonant frequency of S_{22} varies slightly with C_{cpw}. This observation matches the equivalent circuit model analysis in section IV, in which C_{cpw} has a minimal effect on the impedance of Port 1, whereas the impedance of C_{cpw} is loaded into the even mode impedance of Port 2. More importantly, Figure 5-9 shows that S_{21} varies significantly with C_{cpw}. Therefore, C_{cpw} can be utilized to tune S_{22} and S_{21} in the fabrication prototype to mitigate discrepancy between simulation and measurement.

Figure 5-10 describes the S-parameters of the proposed antenna with different values of H_{2m}. It is obvious that S_{22} has a smaller variance compared with the resonant frequency variance of S_{11}. This observation is also consistent with the equivalent circuit model, in which the length of the two thin microstrip lines, $H_{2m,}$ at Port 2 has been loaded heavily into the impedance of Port 1, while for Port 2, these two microstrip lines are quarter-wave transformers used solely for impedance matching.

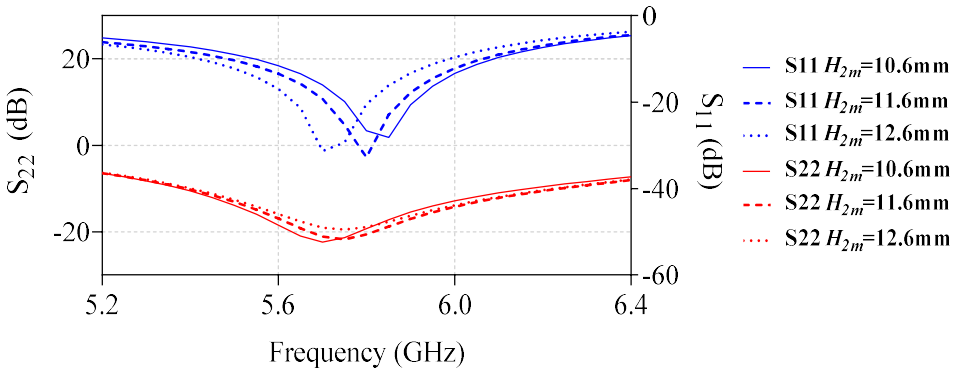


Figure 5-10. Simulated S-parameters with different values of the quarter-wave impedance transformer H_{2m}.

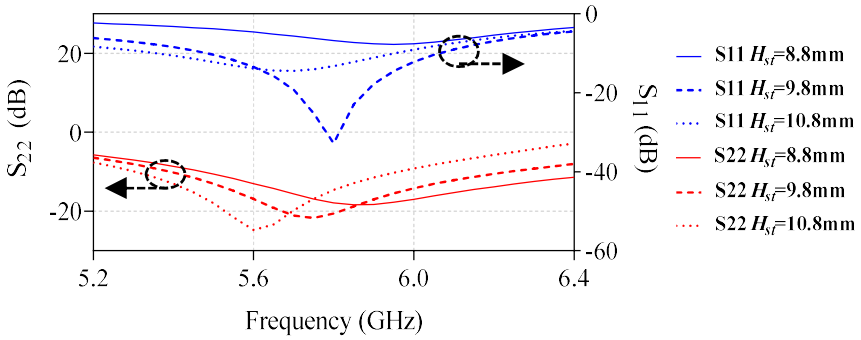


Figure 5-11. Simulated S-parameters with different values of H_{st}.

Figure 5-11 depicts the S-parameters of the proposed antenna with different values of H_{st} in Figure 5-1(a)), or H_{st1} in Figure 5-7(a). From the equivalent circuit models in Figure 5-7 and Figure 5-8, it can be verified that the CPW strongly affects the input impedance of both Port 1 (here, H_{st1} and H_{st2} in the odd mode) and Port 2 (here, H_{st} in the even mode). However, the impedance matching of Port 1 is affected more significantly because the CPW line H_{st1} is connected parallelly with the whole antenna, as shown in Figure 5-7(d). The

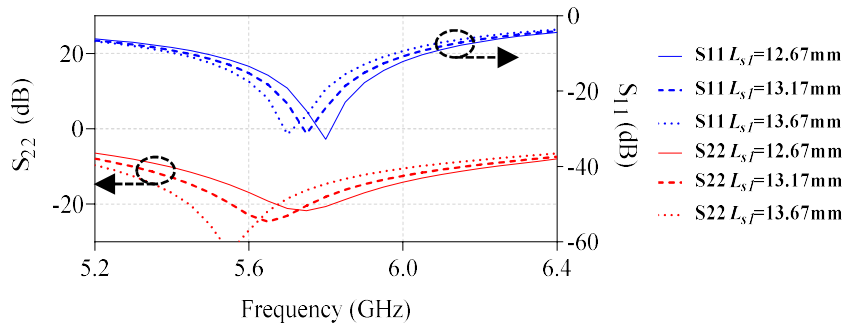


Figure 5-12. Simulated S-parameters with different values of L_{s1}.

lengths of the CPW, namely H_{st}, H_{st1} and H_{st2}, are the most sensitive parameters for both impedance matching and the resonance frequency of both ports.

The longest length L_{s1} (see Figure 5-1(b)) of the stepped slot antenna is also one of the main parameters for optimizing the resonance frequency of both ports (Figure 5-12). As expected, both resonance frequencies of Port 1 and Port 2 shift similarly with each other and inversely with L_{s1}, as shown in Figure 5-12.

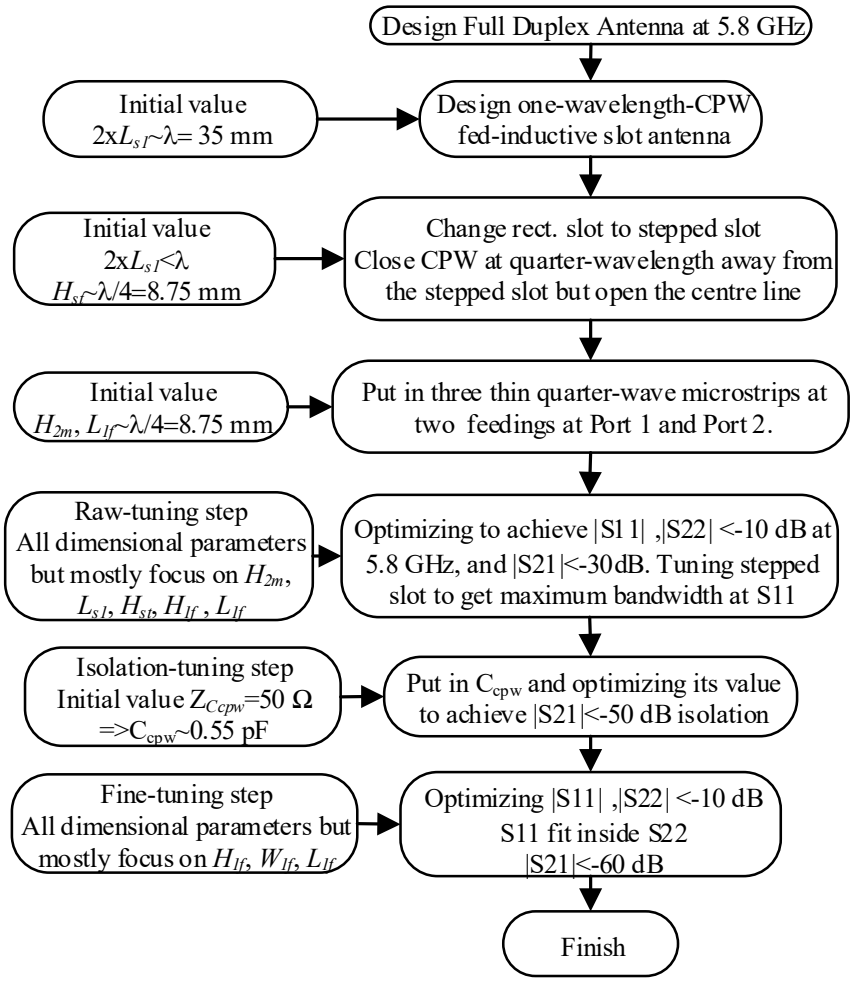


Figure 5-13. Simplified flowchart of design guideline.

The flow chart can be described as follows:

- The first three steps of the flowchart in Figure 5-13 are to calculate the initial values of L_{s1}, H_{st}, H_{2m}, and L_{1f}. The $H_{st} \approx H_{2m} \approx L_{1f} \approx \lambda/4$, $\lambda/4 < L_{s1} < \lambda/2$.
- Raw-tuning step: The parameters H_{2m}, L_{s1}, H_{st}, H_{1f}, and L_{1f} are critical in this step since they determine the impedance matching and resonant frequency (5.8 GHz) of the proposed antenna.
- The isolation-tuning step: Putting C_{cpw} in and optimizing this value to obtain high isolation about 50 dB. Initial value $C_{cpw} \sim 0.55\,pF$ from $Z_{Ccpw} = \frac{1}{2\mathrm{p}fC_{cpw}} = 50\Omega$.
- Fine-tuning step: In this step, S_{11}, S_{22}, and S_{21} are optimized to achieve the best results in terms of bandwidth and isolation. Here, the parameters H_{1f}, W_{1f}, and L_{1f}

are the most important because they can improve the isolation from 50 dB to 60 dB without greatly affecting S_{11} and S_{22}. The reason for this is that the three parameters are at Port 1 and Port 3. They will affect S_{23}, S_{33}, and S_{31} and thus, the coupling coefficient C_{21} (please see equation (5.2).

Based on this procedure, the design can be adapted to different operational frequencies.

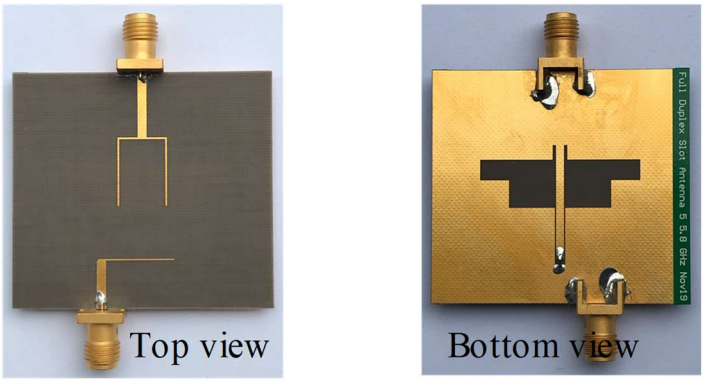


Figure 5-14. Photographs of the fabricated antenna.

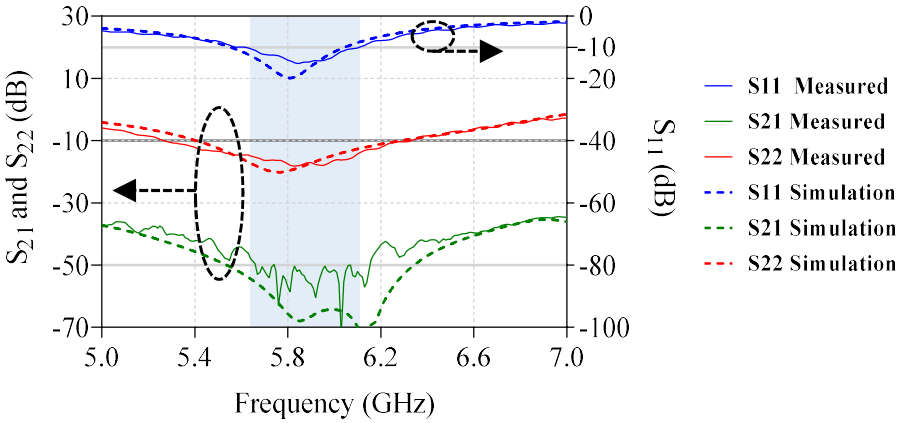


Figure 5-15. Simulated and measured S-parameters of the proposed antenna.

5.2.5 Measurement Results

A photograph of the fabricated prototype is presented in Figure 5-14. The measured results using the Anritsu 37247D network analyzer are shown in Figure 5-15. The working frequency range of Port 1 of the proposed antenna is 5.62 - 6.11 GHz, showing a -10-dB fractional bandwidth (FBW) of 0.49 GHz (8.5%) around the 5.8 GHz center frequency. The working frequency range of Port 2 of the proposed antenna is 5.27 – 6.33 GHz, showing a -10 dB FBW of 1.06 GHz (18.3%) around the 5.8 GHz center frequency. Here, the impedance bandwidth of Port 1 is compromised to achieve a better isolation. The antenna achieves a measured isolation of 57 dB at 5.8 GHz, and the isolation is approximately 50 dB from 5.62 to 6.11 GHz. The S-parameters are measured in a reflective room to take the environmental effects into account.

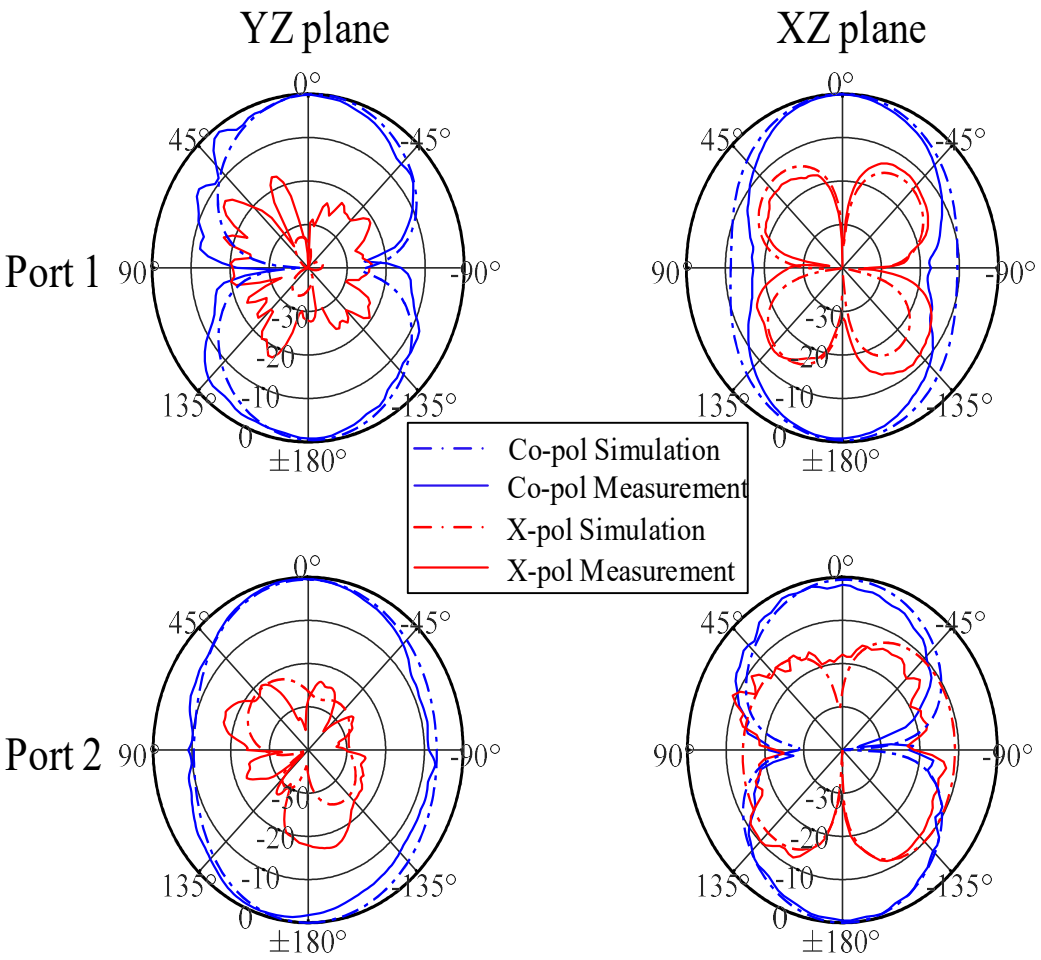


Figure 5-16. Measured and simulated radiation patterns of Port 1 and Port 2 at 5.8 GHz.

The simulated and measured normalized patterns are presented in Figure 5-16, which shows reasonable agreement. The differences between the simulation and measurement at 90° and -90° of xz plane of Port 1 are due to the imperfection of test fixtures, including the effects from the cables and terminated load. The gains across frequency in simulation and measurement are presented in Figure 5-17. The average realized gain of Port 1 is approximately 5.3 dBi while Port 2 is around 6 dBi. The higher gain in Port 2 is due to the fact that even mode excitation has better aperture efficiency with a more uniform field distribution in the slot. The gain differences between simulation and measurement are only about ±0.5 dBi, which is typical for a gain measurement. The antenna has cross-pol discrimination of 25 dB at the broadside of both ports except for Port 2, xz-plane. Furthermore, the two polarizations are orthogonal as the odd mode excited by Port 1 and

the even mode excited by Port 2 generate horizontal and vertical polarization, respectively. Therefore, this antenna can be exploited as a dual-polarized antenna.

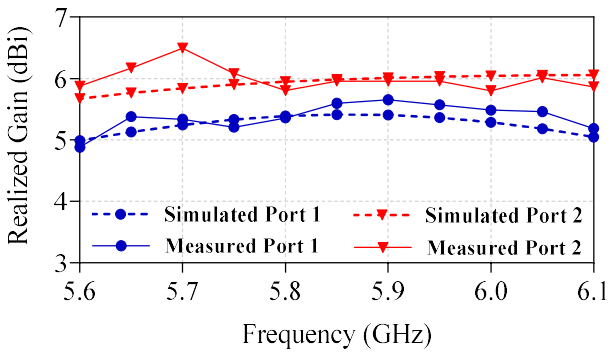


Figure 5-17. Measured and simulated realized gains of Port 1 and Port 2 from 5.6 GHz to 6.1 GHz.

Furthermore, the two polarizations are orthogonal due to the orthogonal feeding from Port 1 and Port 2. Therefore, this antenna can be exploited as a dual-polarized antenna.

Table 5-1. Performance comparison of high isolation antennas.

Ref.	Method	Isolation within bandwidth	Centre frequency (GHz)	Bandwidth (%)	Max. Gain (dBi)	Number of layers	Size (λ^2)
[41]	CPW	30	2.4	27.9 (P1) 35.4 (P2)	5.21	1	1.35 x 1.08
[42]	Coupler & DGS	35	2.4	5.4 (RX) 9.2 (TX)	4	1	1.34 x 0.98
[43]	Coupler	50	2.55	3.7 (P1) 3.7 (P2)	5	2	0.86 x 0.86
[44]	Coupler	40	3.5	2.3 (P1) 2.3 (P2)	12.7	1	4.53 x 1.13
[45]	Decoupling	50	2.45	11(P1) 11(P2)	3	1	>>3.68 x 1.63
[46]	Reflective Term.	40	2.4	8.76 (RX) 8.76 (TX)	8.02	2	1.17 x 1.69
T.W.	**CPW & Reflec. term.**	**50**	**5.8**	**8.5 (RX) 18.3 (TX)**	**6.2**	**1**	**1.2 x 1.07**

Table 5-1 compares the designed antenna and the state-of-art high isolation antennas, in terms of various performance metrics. The proposed antenna shows higher isolation than its ancestors, the CPW antenna [41] and array monopole [42], while its bandwidth is only less than the bandwidth reported in [41]. Overall, the proposed antenna has the highest isolation and the second-best size but with a single layer PCB. The size in the guided wavelength [50] in Table 5-1 is calculated based on the lowest frequency in the operating bandwidth. The antenna in [45] has a high isolation in expense of low gain and an extremely big size due to the decoupling structure.

5.3 Summary

In this chapter, a compact antenna system at 5.8 GHz ISM frequency with IBFD is proposed. Equivalent circuit models are provided to ease the impedance optimization process. The antenna shows a competitive isolation performance compared with the recent antennas while maintaining a small size and a single layer PCB. With this performance, the full-duplex antennas help to achieve full-duplex communication, which represents an attractive option for a high data rate by its potential to double spectral efficiency. The novel isolation technique is proposed without the use of a coupler to achieve device compactness. The proposed full-duplex antenna is designed with a single-layered substrate, thus targeting a low-cost fabrication, like the three harmonic suppression antennas.

6 Conclusion

This chapter summarises the contributions and major findings of this research. This chapter also draws conclusions based on the major findings and outlines the directions for future work. The main goal of the dissertation is to introduce new approaches to address four of the most important features of the RF transceivers' components, namely longer battery lifetime, smaller size or miniaturization, higher data rate, and lower cost. These new approaches are implemented through two of the most crucial parts of a wireless transceiver, which are power amplifiers and antennas. More specifically, they are high linearity CMOS RF power amplifiers, harmonic suppression antennas, and full-duplex antennas.

6.1 Contribution, Major Findings, and Conclusion

6.1.1 High Linearity CMOS Power Amplifier

Chapter 3 presented the first, in-depth physical inside of the design of the CMOS RF PA working at 5.8 GHz ISM frequency, which is a two-stage power amplifier system. The contribution of this chapter is in the systematic design methodology for an RF CMOS PA. First, the technical specifications are derived based on the internal goal of the PA performance. Then, based on the specifications, the two-stage topology with a differential and cascode structure is proposed. The P_{1dB} improvement of a two-stage system compared to a single-stage amplifier is proven using the mathematical equations of a non-linear system. For the proposed high linearity PA, the 1st stage working in class B is combined with the 2nd stage also working in class B for low quiescent current. With the action of the PMOS lineariser, the working class of the 2nd stage will be shifted to class A at high input power to improve linearity, here it is P_{1dB}, compared with its conventional counterpart amplifier. Next, a detailed schematic including transistors, MIM cap, and especially on-chip transmission line transformers or baluns, which are built and simulated in HFSS, are designed based on the topology. The design process of the schematic in Synopsys is represented in block diagrams. The second harmonic short circuit technique is applied to improve P_{1dB} and the saturation power in this schematic.

In addition to the non-linear mathematical analysis in the two-stage system, the major finding of the improvement in P_{1dB} of an RF PA is in the way of using both input and output of the PA to drive the PMOS lineariser while most of the adaptive bias circuits in the

literature use only the input signal. This helps to reduce the DC current consumption and the complexity of the adaptive bias circuit, thus saving design time, size, and cost. Furthermore, this dissertation provides a mathematical analysis of the proposed adaptive bias circuit, thus helping to understand the working principle of the circuit. In this analysis, the Kirchhoff's current and voltage laws are used to derive the relationship between the bias voltage with the other parameters of the circuit in the PMOS lineariser. Then, some parameter studies using the RF Synopsys simulation are carried out to validate this analysis. Thus, with the help of the solid underlying theory, the proposed linearization PMOS circuit can be deployed easily into other PA designs using a different technology process such as 130 nm, 90 nm, and 40 nm and/or at other frequencies.

The layout of the PA is implemented with a specific layout optimization method to reduce parasitic resistance, inductance, and capacitance, thus improving RF performance such as gain and efficiency. Next, the RF PCB schematic and layout are designed, and the PCB is implemented to measure the proposed PA performance.

The measured results of the PA with the linearization PMOS circuit show an output P_{1dB} of 17.5 dBm. The P_{1dB} is compared to other recent works. The improvement in P_{1dB} is around 2.6 dB compared to the conventional PA, which is higher than most of the other works in the literature, which are about 1 to 2 dB. Furthermore, the quiescent current consumption of the whole PA is 44 mA, which is the smallest value compared to the recent works on CMOS PAs. The gain of the proposed PA is a high value of 18 dB while the efficiency (PAE) is a moderate 22.5%. The linearization PMOS circuit has an 10um RMS (root mean square) DC-current consumption, while adaptive bias circuits in other works consume much bigger DC currents, up to some mA.

The PA achieves competitive performance with the lowest DC quiescent current, small chip size and moderate P_{1dB} at the highest frequency and the lowest supply voltage compared to the state-of-the-art PAs in the literature. Furthermore, the proposed PA has common noise immunity due to its differential structure, which is not available in the single-ended structure. With this improvement in P_{1dB}, the PA meets the demand of high linearity PAs in modern wireless communications with a higher peak-to-average power ratio (PAPR) standard. A high PAPR allows a large number of independently modulated subcarriers, thus leading to a high data rate transmission.

6.1.2 Harmonic Suppression Antenna

Chapter 4 proposes three harmonic suppression antennas, the Double Slot Harmonic Suppression Antenna, the Small Size Slot Harmonic Suppression Antenna, and the Wideband Triangle Slot Antenna with Out-of-Band Rejection. All the three antennas work at the ISM frequency of 5.8 GHz using a combination of DGS with other harmonic suppression techniques, namely the MIM capacitor, fringing capacitor, SIR, and thin microstrip line. First, the working principles of the DGS and SIR in harmonic suppression are investigated in detail using the transmission line model. The DGS, when coupled with a microstrip line, works as an inductor in a frequency range lower than its self-resonance frequency. Hence, the DGS can suppress high harmonic frequency components by providing high impedance values at those frequencies. In the meantime, the DGS maintains low impedance at the operating frequencies and thus has little impact on the performance of the modified antenna at these frequencies.

The SIR, on the other hand, shifts the high harmonic components to higher harmonic frequencies, thus proving suppression at these frequencies. In addition to the harmonic suppression capability, the SIR also provides size reduction, however at the expense of smaller bandwidth. Importantly, the bandwidth of the slot antenna in a uniform rectangular and SIR shape is self-derived using lumped-element equivalent circuits combined with the transmission line model. The contribution of this section is that the bandwidth of a uniform rectangular slot antenna, which follows linearly with its slot line impedance, can be proven using mathematical equations and HFSS simulation. Similarly, the bandwidth of an SIR slot antenna is inversely proportional with the impedance ratio K in a linear manner. Furthermore, the K value, which is the main factor of an SIR structure, significantly affects the harmonic suppression capability. Therefore, the K value must be chosen to balance between the bandwidth goal and the harmonic suppression goal.

Other components such as the MIM capacitor, fringing capacitor, and thin microstrip line act like a lumped capacitor and a lumped inductor in a low pass filter, which can be proven using electromagnetic theory and verified by HFSS simulation, thus suppressing higher order harmonics. The MIM capacitor can help to improve bandwidth by more than 1% in a narrow slot antenna while the fringing capacitor narrows the bandwidth. One of the major findings in this dissertation is that the thin microstrip line can improve the bandwidth of a triangle slot antenna by exciting another resonant frequency near the existing operating frequencies.

The size of the Double Slot Harmonic Suppression Antenna is reduced by 8.4% compared to that of its conventional counterpart rectangular slot antenna while the

bandwidth is reduced by only 2.5%. The size of the Small Size Slot Harmonic Suppression Antenna is reduced by 25% compared to the conventional rectangular slot antenna at the expense of nearly half the bandwidth, from 10.2% to 5.5%. However, these bandwidths still meet the bandwidth specification of 200 MHz for our industrial project for AM modulation. The major finding in relation to these two narrowband antennas is that the insertion of SIR reduces the size while improving harmonic suppression capability. In addition to return loss, the simulated radiation patterns of the two narrow slot antennas at 5.8 GHz and the second and the third harmonic frequencies are used to validate the harmonic suppression capability.

In the Wideband Triangle Slot Antenna with Out-of-Band Rejection, the measured radiation pattern at 5.8 GHz of the proposed antenna is similar to that of the conventional antenna, meaning the harmonic supersession structures do not affect the antenna's performance at this frequency. The measured bandwidth of the proposed harmonic supersession antennas is the best performance compared to the recent harmonic supersession antennas in the literature. The major finding is that the triangle slot shape can be impedance-matched to operate in a very wide band using harmonic supersession structures, which are the DGS and the thin microstrip line. The bandwidth increases from 20% of the conventional antenna to 83% of the proposed antenna. The miniaturization of ground size is achieved by a simple cut and adding matching elements. Furthermore, the small width of the ground surrounds the slot reduces the overall size of the antenna. The size of the proposed wideband antenna is thus reduced by 60% compared to the reference rotated square slot antenna. The final ground of the antenna is 0.46 x 0.46 in wavelength unit, which is the second-smallest size among the state-of-the-art harmonic suppression antennas. The minimum S_{11} of 1.2 dB in the rejection band is the second lowest among recent works. The rejection band is from 1.15 f_h - 3.38 f_h where f_h is the highest frequency in the operating frequency band, which is 8.81 GHz. This rejection bandwidth is also the second largest in recent harmonic suppression designs.

In conclusion, the insertion of harmonic suppression structures into the three antennas does not affect the radiation patterns at the operating frequencies. Moreover, the insertion helps reduce the size of all three antennas. However, the operating bandwidth of the two narrowband slot antennas is reduced whereas the operating bandwidth of the wideband triangle slot antenna is significantly improved. All three antennas achieve very strong out-of-band rejection which have no bumps or resonance at the rejection bandwidth. Furthermore, the underlying theory of harmonic supersession structures is investigated in

detail to to enable a deeper understanding of the suppression mechanism. Therefore, it can be said that the three antennas achieve the miniaturization goal as well as the harmonic suppression target. The strong out-of-band rejection improves the efficiency of active circuits, thus resulting in longer battery lifetime. In addition, the signal-to-noise ratio improves with this good performance of rejection, leading to a higher data rate.

6.1.3 Full-Duplex Antenna

Chapter 5 proposes a full-duplex antenna system working at 5.8 GHz. The isolation between even mode and odd mode in a CPW antenna is investigated theoretically using the incident and reflection matrix of a CPW-slotline tee. Then, the odd mode is supplied to the CPW-slotline tee by the coupling between a transverse microstrip line and the CPW. The even mode is provided by a T-junction microstrip power divider. The isolation between the even mode and odd mode is then verified by HFSS electric field simulation, which is around 30 dB. Next, a lumped capacitor is used to boost the isolation to more than 60 dB in the simulation. The cancellative reflection of a capacitor is also proven by the coupling coefficient equation using S-parameters of a three-port network and is verified by the HFSS electric field simulation.

Importantly, the equivalent transmission line circuit models in the even and odd modes are derived to gain a deeper theorical insight into the design and to assist the optimization process. To the best of our knowledge, none of the existing works on full-duplex antennas provide equivalent transmission line models for impedance and isolation optimization. The measured isolation performance of the proposed antenna system, which is 50 dB, is the highest compared with recent works on full-duplex planar antennas. The contribution of the proposed technique in this high isolation antenna is that it does not use any coupler, thus it can achieve a small size. The size of the antenna is 1.2 x 1.07 in wavelength units, which is the second best among recent works. The fabricated PCB has only one layer, hence it has a low profile and a low cost.

The proposed full-duplex antenna has a high isolation of 50 dB, thus helping to achieve full-duplex communication, which represents an attractive option for a high data rate by its potential to double spectral efficiency. The antenna is also small in size, thus satisfying the miniaturization goal. The antenna has a single layer PCB, which helps reduce the fabrication cost.

6.1.4 Summary

In summary, the works on CMOS PAs, harmonic suppression antennas, and full-duplex antennas use a mathematical platform developed in this study, to help understand and adjust the most sensitive parameters and factors of each design and hence, assist the design process. In addition, the overall performance, in terms of size, bandwidth, gain, isolation and rejection performance of the harmonic supersession and full-duplex antenna designs are among the best, compared with recent works in the same field. In the linearity PA design, the P_{1dB} improvement and quiescent current performance of the proposed PA is the best compared to the work in the literature. This performance results in the goals of longer battery lifetime, smaller size or miniaturization, higher data rate, and lower cost being met.

Lastly, the comprehensive literature review in Chapter 2 on the recent techniques for developing CMOS PAs, harmonic suppression antennas, and full-duplex antennas provides a deeper understanding of the advantages and disadvantages of these techniques. Based on this review, feasible solutions are proposed to mitigate the existing problems, namely their large size, small bandwidth, low linearity, weak out-of-band rejection and low isolation, etc.

6.2 Future Work

The following issues need to be addressed in the future to further enhance the high linearity CMOS PAs, harmonic suppression antennas and full-duplex antennas proposed in this thesis so that the outcomes of this research can be enhanced further to be used commercially for RF components.

6.2.1 High Linearity CMOS PA

The PA is designed with a considerable improvement in P_{1dB} while maintaining gain, quiescent current, and efficiency. However, there are areas that can be developed further to provide an industry-ready product. Future research for the CMOS PA may include the development of the PA in an RF transceiver. This will result in a more fine-grained design and performance trade-off in terms of size, current consumption, and output power. The number of voltage sources will be reduced by designing internal voltage sources for the three biasing voltages, one for the 1^{st} stage biasing, one for the 2^{nd} stage amplifier biasing, and one for PMOS biasing. Furthermore, in this thesis, the single tone signal is used to simulate the amplifier and measure the P_{1dB}. Future work will focus on using modulated signals and a good extension of this would be to make further improvements to IMD3 and IMD5. In addition, the amplifier is designed using the 180 nm TSMC process which was

commercialized during the period 1998–2000. The usefulness of this technology in relation to high frequency application is limited by the low maximum cut-off frequency and the maximum oscillation frequency of the constituting transistors. The performance in gain and P_{1dB} at 5.8 GHz of the proposed PA are therefore not competitive compared to similar works at smaller technology process. The CMOS PA can be re-designed using a newer process such as 40 nm at 5G frequency such as 30 GHz or 77 GHz to achieve better linearity and gain performance with a smaller size.

6.2.2 Harmonic Suppression Antenna

The proposed wideband harmonic suppression antenna satisfies some of the most important requirements: low cost, single layer, small size, wide bandwidth, and out-of-band rejection. However, there are areas that can be developed further to provide an industry-ready product. Future research on the Harmonic Suppression Antenna may include the development of the antennas at 5G frequency such as 30 GHz or 77 GHz. At this frequency, the antenna is small enough to be embedded in monolithic microwave integrated circuit (MMIC) substrates to achieve a system on chip design, thus reducing size and cost.

The antenna's substrate, a high frequency laminate Taconic TLY-5 which is an expensive material, can be replaced with less expensive and more commercially available ones, such as FR4 if the antenna is designed at the lower frequency range of 5G such as 2.5/3.5 GHz. The antenna can be integrated with active power amplifier circuits or active oscillator circuits to verify the reduction of higher harmonic components in these circuits.

6.2.3 Full-duplex Antenna

The in-band full-duplex antenna is a new area of research. The full-duplex antenna is proposed in this thesis with reflective termination theory, designed using HFSS simulation, and validated by the measurement results. The proposed antenna satisfies some of the most important requirements: low cost by using a single layer with a small-sized PCB, moderate bandwidth, and very high isolation. However, further investigation is needed for a more competitive performance. The current design of the full-duplex antenna has an 8.5 % common bandwidth which may be not large enough for wideband applications. Therefore, future research on the full-duplex antenna may include a wider bandwidth antenna while keeping the high level of 50 dB isolation. In addition, the isolation of all the planar full-duplex antennas in the state-of-the-art antennas cannot break through the milestone 50 dB. This is because the unsymmetrical design, leaked surface current and electromagnetic field

increase the mutual coupling between the RX and TX antennas. The noisy environment where the measurement takes place also contributes to the low isolation. Therefore, extensive research works on theory should be done to solve this bottleneck isolation. Moreover, the antenna can be put in a multi-element array antenna to achieve very high gain, which meets the needs of radar and base station designs. The cost of the antenna is considerable high because the substrate is the high frequency and expensive Taconic TLY-5 material. Future research can investigate the use of less expensive and commercially available substrates. The size of the proposed antenna can be reduced further to meet the current trend of miniaturization using different antenna structures, in addition to the CPW and slot structures. Finally, the antenna should be embedded into MMIC substrates to be an on-chip antenna if the millimetre-waves of 5G are expected to be the operating frequencies.

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