Engineering the Spin-Orbit Interaction in Surface Conducting Diamond with a Solid-State Gate Dielectric

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ABSTRACT:

Hydrogen-terminated (H-terminated) diamond, when surface transfer doped, can support a sub-surface two-dimensional (2D) hole band that possesses a strong Rashba-type spin-orbit interaction. By incorporating a V_2O_5/Al_2O_3 bilayer gate dielectric in a diamond-based metal-oxide-semiconductor (MOS) architecture, metallic surface conductivity can be maintained to low temperature, avoiding the carrier freeze-out exhibited by devices with an Al_2O_3 gate dielectric alone. Hole densities up to 2.5×10^{13} cm^{-2} are achieved by electrostatic gating of the device and the spin-orbit interaction strength can be tuned from 3.5 ± 0.5 meV to 8.4 ± 0.5

meV, with a concurrent reduction in the spin coherence length from 40 ± 1 nm to 27 ± 1 nm. The demonstration of a gated device architecture on the H-terminated that avoids the need to cycle the temperature, as is required for ionic liquid gating protocols, opens a pathway to engineering practical devices for the study and application of spin transport in diamond.

KEYWORDS: hydrogen-terminated diamond, surface conductivity, spin-orbit interaction, Rashba effect, quantum coherent backscattering

Diamond is a wide-band gap (5.5 eV) semiconductor endowed with a range of desirable electronic properties. [1] Amongst them is the negative electron affinity possessed by the diamond surface when hydrogen-terminated (H-terminated) which, when interfaced with suitable surface acceptors such as atmospheric adsorbates, [2] or solid-state acceptors with high electron affinity, such as MoO_3 and V_2O_5 [3 ~ 10] induces a *p*-type surface conductivity. This arises from a two-dimensional (2D) hole accumulation layer which forms as a consequence of spontaneous electron transfer from the diamond valence band into electron-accepting states of the adsorbates, a process known as surface transfer doping. Significant progress has been made in engineering the surface conducting (SC) diamond for electronic devices. [11] In particular, several breakthroughs have been achieved on diamond-based metal-semiconductor field-effect transistors (MESFETs) [1, 12 ~ 14] and metal-oxide-semiconductor field-effect transistors (MOSFETs) [15 ~ 17], motivated by the huge potential of surface conducting diamond for high-power, high-frequency transistors. In these MOSFETs architectures, a single aluminum oxide (Al_2O_3) layer deposited via atomic layer deposition (ALD) is used as a gate dielectric layer. Through this method, the operation of H-terminated diamond MOSFETs has been demonstrated at both room temperature and high temperature (400 °C). [17]

Recently, an emerging interest in exploring the quantum transport properties of the sub-surface 2D hole band has been made possible through improvements in the quality of H-terminated surfaces. The observation of Shubnikov-de-Haas in air-doped H-terminated diamond, [18, 19] and phase-coherent backscattering effects in both air-doped and transition-metal-oxide-doped H-terminated diamond, [20, 21] have yielded direct evidence of the 2D Fermi liquid nature of the sub-surface hole band. Comprehensive magnetotransport measurements performed in the limit of low applied magnetic field have, through the observation of quantum coherent backscattering in the form of weak localization (WL) and weak antilocalisation (WAL), shown that the 2D hole band possesses a strong spin-orbit interaction (SOI), [20, 21] and permitted an evaluation of the gyromagnetic ratio. [22] The spin-orbit interaction arises through the Rashba effect as a result of the highly asymmetric quantum confinement potential at the diamond surface. By engineering the asymmetry of the potential well with an ionic liquid gate, the SOI has been shown to be tunable over a five-fold range. [23] This suggests that surface conducting diamond has potential for the development of devices in which the hole spin can be used to transport information. However, the inclusion of ionic liquid in the device architecture presents significant challenges to future device integration and process flexibility. In addition, to operate devices at low temperature alternative device architectures are necessary which preclude the need to warm the device in order to vary the gate bias as is necessary in ionic liquid gating protocols.

In this work, we demonstrate the operation of a surface conducting diamond all-solid-state MOSFET in which the SOI can be modulated using an electrostatic gate at low temperature. The device incorporates a V_2O_5/Al_2O_3 dielectric bilayer which gives a significantly higher source-drain current compared to devices with a single Al_2O_3 dielectric layer. As a result, for the V_2O_5/Al_2O_3 bilayer device, surface conductivity is found to persist to low temperature

which is not achievable in Al/Al_2O_3/H-diamond MOSFETs due to carrier freeze-out at low temperature. Low temperature magnetotransport is used as a powerful tool to evaluate the SOI in the 2D hole band as a function of gate bias.

Prior to the fabrication of devices, commercial type-IIa (001) single crystal diamond samples (*Element Six*) were cleaned by boiling in an acid mixture (NaN_3 and H_2SO_4) at 500 °C for 45 minutes to remove metallic and organic adsorbates. The sample was then treated in a microwave hydrogen plasma operating with a power of 1500 W at 850 °C for 10 minutes, rendering the surface H-terminated. Hall bar devices (width 50 μm and length 200 μm) were fabricated on the H-terminated surface using standard photolithographic and lift-off techniques as reported previously [20, 23]. Active, H-terminated Hall bar regions were formed by capping the surface with a protective photoresist layer (Az nlof 2020) and oxygen-terminating surrounding regions of the surface were formed via exposure to an oxygen plasma operating at 50 W. Ohmic contacts were formed using palladium (Pd) (100nm) which shows significantly lower contact resistance than the commonly used Ti/Pt/Au contacts, [24] and Ohmic behavior at cryogenic temperature. [25] A V_2O_5 adlayer (thickness 5 nm) was then selectively deposited (with a deposition rate of 1 Å/min) via evaporation in ultra-high vacuum through a shadow mask onto the Hall bar channel of some of the devices. Following deposition of the V_2O_5 adlayer, a 20 nm Al_2O_3 dielectric layer was deposited using ALD on the entire surface with the sample at a temperature of 150 °C by alternately supplying of trimethylaluminum and H_2O. Finally, an aluminum (Al) gate electrode was defined on each device by standard photolithographic processing. Using this fabrication approach devices with two different dielectric adlayer structures, an Al_2O_3 single-layer dielectric and a V_2O_5/Al_2O_3 bilayer dielectric (Figure 1c), were fabricated on the same diamond substrate (Figure 1c).

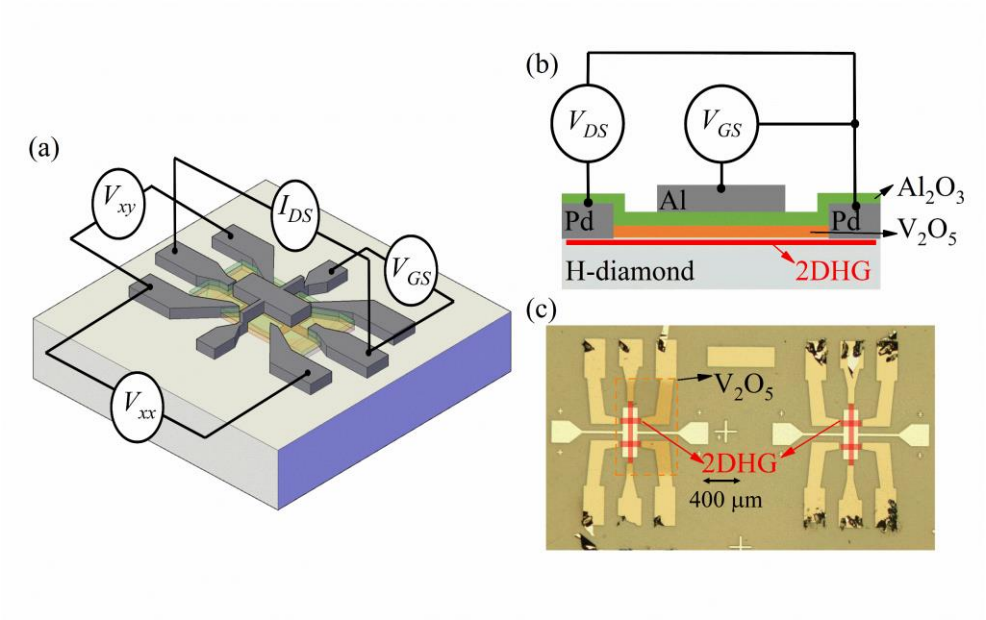

Figure 1: (a) Schematic representation of a gated Hall bar illustrating the electrical connections used for magnetotransport measurements; (b) Schematic cross-section of a gated Hall bar illustrating the V_2O_5 and Al_2O_3 dielectric bilayer; (c) Optical image of the device, the orange dashed area highlights the V_2O_5 adlayer; the red areas illustrate the regions of the H-terminated Hall bars.

Current-Voltage (*I-V*) characteristics of the fabricated Hall bar devices (see Figure 1b) were measured in the temperature range 80 K – 4 K using a Janis SHI-950 cryogen-free refrigerator. Two Keithley 2450 source-meters were used to apply a voltage between drain and source contacts (V_{DS}), and gate and source contacts (V_{GS}), and to monitor the drain-source current (I_{DS}). Magnetotransport measurements (Figure 1a) were performed using a Leiden cryogenics dry dilution refrigerator with a superconducting vector magnet (9-1-1 T). One Keithley sourcemeter was employed as a current source which simultaneously characterized the longitudinal voltage V_{xx} in order to determine the corresponding resistivity ρ_{xx} as a function of temperature. In parallel, the Hall voltage V_{xy} was measured using an Agilent 34410A multimeter to determine the transverse resistance, R_{xy}.

The Hall characteristics of the two devices with different dielectric structures were initially measured at room temperature with zero gate bias. For the device with a single Al_2O_3 dielectric layer, the introduction of the dielectric and gate electrode cause an increase in the channel resistance relative to that of the pristine H-terminated diamond surface. As a consequence, the device requires the application of a negative gate bias in order to operate. In contrast, for the device with the V_2O_5/Al_2O_3 dielectric bilayer a hole density of 7×10^{12} cm^{-2} was measured at room temperature; the V_2O_5 acceptor layer acting to maintain a high hole density even in the absence of a gate bias [26], as a result of its superior surface transfer doping efficiency [8, 27]. Figure 2 shows corresponding source-drain output *I-V* curves, measured at 80 K and 4 K, in response to an applied gate bias. For the device with a single Al_2O_3 dielectric layer modulation of I_{DS} as a function of V_{GS} is observed at 80 K (Figure 2a) with typical transistor output characteristics; I_{DS} can be tuned up to 3.5 µA with a gate bias V_{GS} = -3.5 V. However, the same measurements performed at 4 K yield a I_{DS} no greater than 0.05 nA despite the application of the gate bias, indicating carrier freeze-out and preventing operation of this device as a MOSFET at low temperature. The carrier freeze-out is likely to be caused by interface defects induced by the Al_2O_3 ALD deposition, which would serve to trap charge carriers at low temperature. The device with an Al_2O_3/V_2O_5 bilayer exhibits a significantly improved performance, with I_{DS} several times higher for a given V_{DS} (I_{DS} = 18 µA for V_{GS} = -3.5 V) and the Hall bar channel remains conductive at low temperature permitting modulation with the gate. The addition of the V_2O_5 layer prior to deposition of the Al_2O_3 is thus indispensable in preventing carrier freeze-out and permits study of the transport behaviour in the 2D hole band at low temperature. The exceptionally high electron affinity (6.3 eV) of V_2O_5 places its conduction band edge well below diamond valence band maximum, resulting in a negative activation energy.

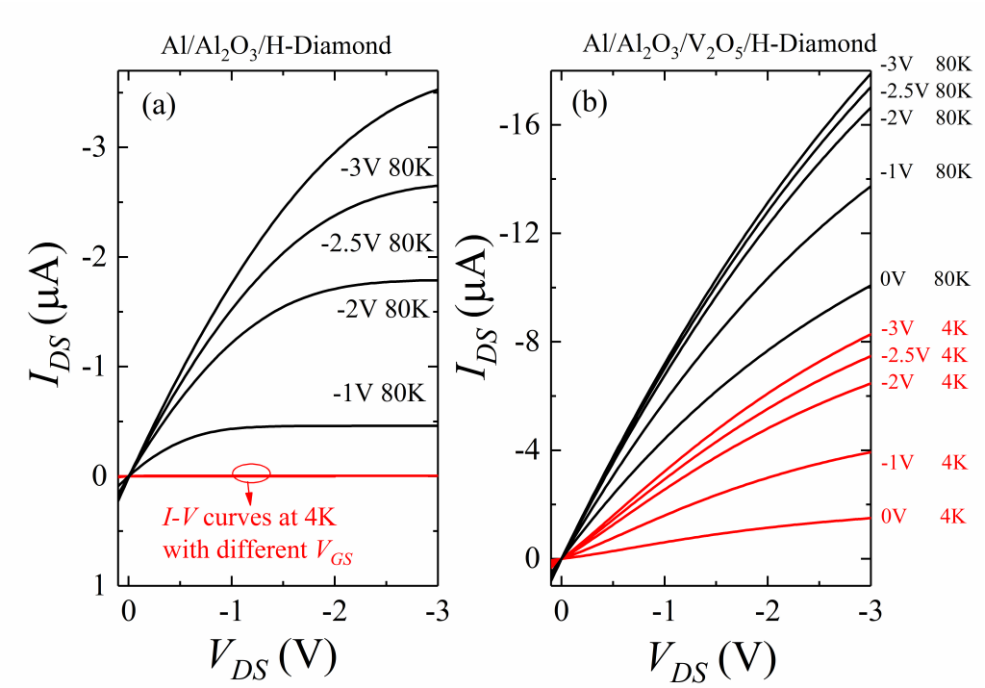

Figure 2: Comparison of the source-drain *I-V* output curves for devices with different dielectric structures: (a) device with a single Al_2O_3 dielectric layer; (b) device with an Al_2O_3/V_2O_5 bilayer.

We now turn to the transport measurements at temperatures of 8 K and below, focusing on the device with an Al_2O_3/V_2O_5 dielectric bilayer for which a metallic surface conductivity persists at low temperature. As we discuss elsewhere, [20] the temperature dependence of the 2D surface conductivity can be described through quantum corrections to the Drude conductivity (σ_D) arising from hole-hole interactions (HHI) and phase-coherent backscattering in the form of weak localization (WL) and weak anti-localization (WAL). [28 ~ 30] The corresponding corrections, $\delta\sigma_{HH}$ and $\delta\sigma_{BS}$, to σ_D can be treated independently to give a 2D longitudinal conductivity of the form $\sigma_{xx} = \sigma_D + \delta\sigma_{BS} + \delta\sigma_{HH}$. The two corrections have very different responses to an applied magnetic field, making it possible to separate them unambiguously. The HHI affects the Hall resistivity through a $\sim\ln(T)$ correction, while phase coherent backscattering does not. Phase coherent backscattering has a distinctive dependence on magnetic field, while HHI are independent of the field.

The HHI correction to the Drude conductivity takes the form, [31]

$$\delta\sigma_{HH} = K_{HH} G_0 \ln\left(\frac{k_B T \tau}{\hbar}\right), \quad (1)$$

where $G_0 = e^2/\pi h$, and K_{HH}, k_B, T, and h are the HHI strength, Boltzman constant, temperature, and the Planck constant, respectively. The transport relaxation time, τ, is given by $\tau = m^* \sigma_D / e^2 n_{2D}$, where $n_{2\mathrm{D}}$ is the areal hole density, $m^* = 0.208\, m_0$ is the in-plane heavy hole mass, [20] and e is the elementary charge.

The HHI correction is evaluated following the approach of Goh *et.al.* [31] which checks the validity of an initial estimate of K_{HH} (see Supplementary material) by subtracting $\delta\sigma_{HH}$ from the Hall resistance, $R_{xy}(B)$. If the value is correct, all $R_{xy}(B)$ traces taken at different temperatures will collapse onto the same Hall slope. The K_{HH} values are subsequently systematically adjusted and $\delta\sigma_{HH}$ is recalculated until the correction when applied to $R_{xy}(B)$ satisfies this requirement as shown in Figure S2; the corresponding final values of K_{HH} are listed in Table S1 in the Supplementary material. The carrier density of holes was then derived from the slope of the HHI-corrected traces using the expression $n_{2D} = B / \rho_{xy} e$. The hole density was found to vary linearly with gate bias as illustrated in Figure 4a and is tunable from 1.2×10^{13} cm^{-2} to 2.5×10^{13} cm^{-2}. From the slope of n_{2D} vs. V_{GS}, a gate capacitance of 0.42 μF/cm^2 is calculated which is comparable with literature values obtained for surface conducting diamond devices incorporating a MoO_3 dielectric layer operating at room temperature. [32]

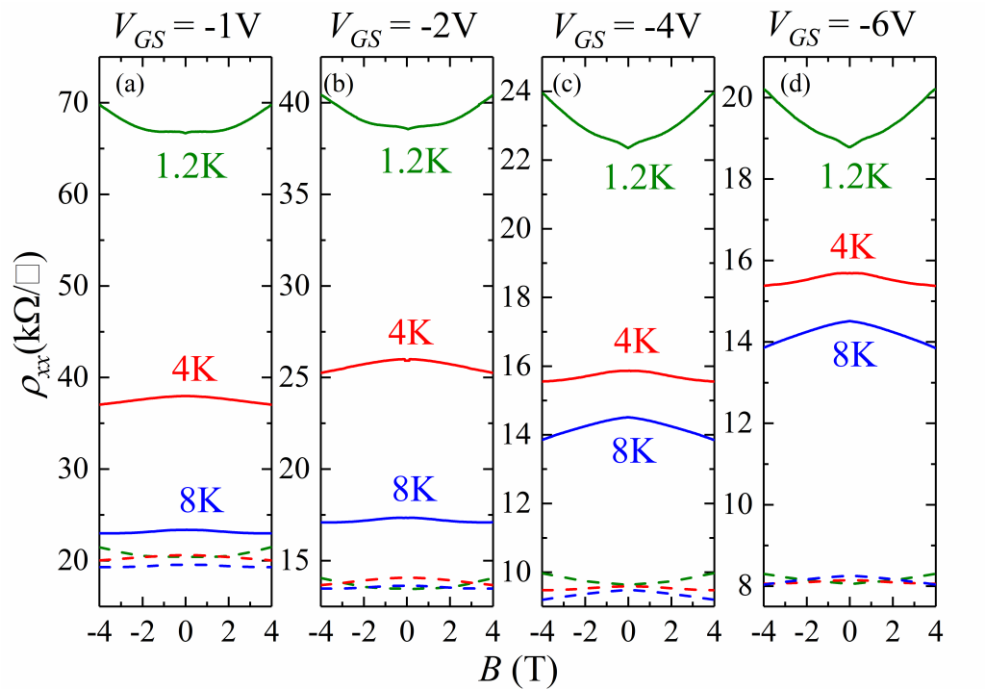

Figure 3: Longitudinal resistivity, ρ_{xx}, plotted as a function of magnetic field at different gate biases, before (solid lines) and after (broken lines) HHI removal.

Having accounted for the HHI correction to the Drude conductivity through its effect on $\rho_{xy}(B)$, we now turn to consider the magnetoresistivity, $\rho_{xx}(B)$. Figure 3 shows uncorrected and HHI-corrected $\rho_{xx}(B)$ curves measured over the temperature range 1.2 K to 8 K for each gate bias. In each case the $\rho_{xx}(B)$ curves exhibit characteristic cusps around B = 0 T which are typical of 2D electronic systems and arise from corrections to the Drude conductivity due to phase coherent backscattering. At 4 K and 8 K a negative magnetoresistivity around B = 0 T due to WL. At 1.2 K, a positive magnetoresistivity cusp emerges due to WAL which is a signature of strong SOC in the 2D hole band. [20] The evolution from WL to WAL arises because the phase coherence length, which determines the size of backscattering loops, increases as the sample is cooled. At low temperature the phase coherence length exceeds the spin coherence length so that the hole spin precesses as the carriers are backscattered. In order to quantify the WAL behaviour and extract information relating to the SOC, the change in low-field

magnetoconductivity, $\Delta\sigma = \sigma(B) - \sigma(0)$ at different gate biases is considered. Figure 4b shows experimental $\Delta\sigma$ curves measured at 1.2 K for each gate bias: -1 V (black); -2V (blue); -4 V (orange) and -6 V (green). The relative intensity of the WAL cusp increases considerably with gate bias, indicating an increase in SOC with gate bias.

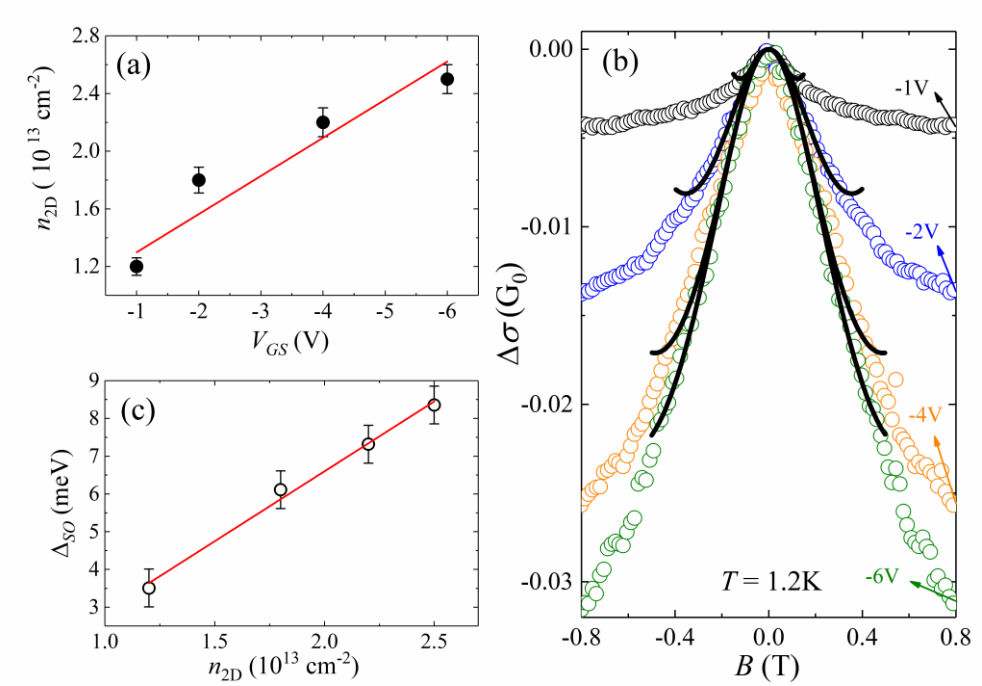

Figure 4: Transport behaviour for the device with an Al_2O_3/V_2O_5 dielectric bilayer. (a) Hole density, after HHI correction, as a function of applied gate bias; (b) Change in magnetoconductivity, $\Delta\sigma = \sigma(B) - \sigma(B = 0)$ in units of $G_0 = e^2/\pi h$, measured for different gate bias at 1.2 K. Open circles represent the experimental data; the solid lines are fits to eqn. (2); (c) Variation of the spin-orbit interaction, Δ_{SO}, as a function of hole density.

The measured magnetoconductivity curves are compared to the 2D localization theory developed by Hikami: [30, 33]

$$\frac{\Delta\sigma}{G_0} = -\left\{ \begin{array}{l} \psi\left(\frac{1}{2}+\frac{B_\phi + B_{SO}}{B}\right)+\frac{1}{2}\cdot\psi\left(\frac{1}{2}+\frac{B_\phi + 2\cdot B_{SO}}{B}\right)-\frac{1}{2}\cdot\psi\left(\frac{1}{2}+\frac{B_\phi}{B}\right) \\ -\ln\left(\frac{B_\phi + B_{SO}}{B}\right)-\frac{1}{2}\cdot\ln\left(\frac{B_\phi + 2\cdot B_{SO}}{B}\right)+\frac{1}{2}\cdot\ln\left(\frac{B_\phi}{B}\right) \end{array} \right\} \quad , (2)$$

where ψ is the Digamma function and B is the applied magnetic field. $B_\phi = \hbar/\left(4eD\tau_\phi\right)$ and $B_{SO} = \hbar/\left(4eD\tau_{SO}\right)$ are the characteristic phase- and spin- fields, where τ_ϕ is the phase coherence time, τ_{SO} the spin coherence time, and D the diffusion constant. Fits to theory which use B_ϕ and B_{SO} as variable parameters, illustrated by the solid lines in Figure 4b, satisfactorily reproduce the experimental data in the diffusive magnetic field regime. From the values of B_{SO} derived from fitting, the corresponding values for the spin coherence length were evaluated using $L_{SO} = \left(\hbar/4eB_{SO}\right)^{0.5}$. The dependence of both B_{SO} and L_{SO} on the hole density (after HHI correction) is illustrated in Figure S3. B_{SO} is observed to increase linearly with hole density, and it follows that L_{SO} is proportional to the inverse square root of the hole density, varying from 40 ± 1 nm to 27 ± 1 nm as the hole density is increased. This reduction in L_{SO} gives rise to the observed increase in intensity of the WAL cusp with gate bias, as evident in Figure 4b.

Finally, from the derived values of B_{SO} we calculate the key spin parameters $\tau_{SO} = \hbar/\left(4eDB_{SO}\right)$ and the SOI strength, $\Delta_{SO} = \hbar/\left(2\tau\tau_{SO}\right)^{0.5}$.[20] Here, $\tau = \sigma_D m^*/n_{2D}e^2$ is the transport relaxation time and the diffusion constant is given by $D = l^2/2\tau$, where $l = \left[\left(2\pi\right)^{0.5}\hbar\sigma_D\right]/\left[e^2\left(n_{2D}\right)^{0.5}\right]$ is the hole mean free path. Values of all key parameters are listed in Table S1. The spin coherence length is found to increase with decreasing hole density in the range 1.5 to 11.0 ps, consistent with previous measurements on air-doped surface conducting diamond devices. [23] The dependence of Δ_{SO} on the hole density is illustrated in

Figure 4c, which shows that the SOI can be tuned from 3.5 ± 0.5 meV to 8.4 ± 0.5 meV by varying the applied gate bias. The tuning dynamic range is found to be smaller than that achieved in H-terminated diamond devices using an ionic liquid gate, [23] because of the lower capacitance compared to the ionic liquid gated Hall bar devices as a result of limited hole density tuning dynamic range, but the Al_2O_3/V_2O_5 bilayer dielectric avoids the need to warm the device in order to change the applied gate bias as is the case for ionic-liquid gating protocols and therefore provides an avenue to engineering practical spin transport devices. In principle, the dynamic range of Δ_{SO} can be increased by exploiting thinner dielectric layers, simultaneously replacing the Al_2O_3 with an alternative material with a higher dielectric constant, such as HfO_2.

In summary, H-terminated diamond MOSFET devices with metallic surface conductivity at 1.2 K have been demonstrated using an Al_2O_3/V_2O_5 bilayer dielectric gate architecture, the V_2O_5 layer acting as a surface acceptor which avoids the carrier freeze-out exhibited in devices with an Al_2O_3 layer alone. By applying a gate bias up to -6 V, the hole density and spin-orbit interaction are modulated at low temperature. The SOI strength can be tuned from 3.5 ± 0.5 meV to 8.4 ± 0.5 meV, with a concurrent reduction in the spin coherence length from 40 ± 1 nm to 27 ± 1 nm. The ability to tune the spin-orbit coupling at low temperature, along with the fact that spin relaxation occurs on an experimentally accessible length scale, opens an avenue towards the development of practical devices for the study and application of spin transport in diamond.

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AUTHOR CONTRIBUTIONS

The manuscript was written through contributions of all authors. All authors have given approval to the final version of the manuscript.

DATA AVAILABLE ON REQUEST FROM THE AUTHORS

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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